|| Jai Sri Gurudev ||

ADICHUNCHANAGIRI INSTITUTE OF TECHNOLOGY

(Affiliated to VTU, Accredited by NBA) CHIKKAMAGALURU-577102, KARNATAKA, INDIA.

Department of Electronics and Communication Engineering

Report on

FPGA & EMBEDDED SYSTEM DESIGN FLOW ON ZYNQ USING VIVADO

FDP Description: Five days Faculty development program on FPGA and Embedded System Design Flow on ZYNQ using Vivado was conducted by department of ECE, AIT Chikkamagaluru from 03.02.2020 to 07-02-2020. The objectives of this FDP is to enhance the knowledge in the field of VLSI, Verilog and Understand the design of Embedded system.

Resource Persons:

Dr. Shashidara K.S, Professor , ECE Dept., NMIT, Sujeeth Kumar, Application Engineer and Vijendra V, Application Engineer, Bangalore – 560034.

Signature of the Coordinator

Signature of the HOD

Dept. of Electronics & Communication Engg.
Adichunchanagiri Institute of Technology
Chikmagalur - 577 102

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING
ADICHUNCHANAGIRI INSTITUTE OF TECHNOLOGY
JYOTHINAGAR, CHIKMAGALUR - 577 102
(Affiliated to V.T.U, Belgaum Recognized by A.I.C.T.E, New Delhi)
(Accredited by N.B.A, New Delhi, ISO 9001: 2008 Certified)
Email: np_sreenivasa@yahoomail.com, Ph: 08262-220514, 220444, Tel Fax: 08262-220063

Ref No: AIT / E&C /01/2019-2020 **Date:** 31-01-2020

Dear Dr.Shashidhara K S

Greetings from AIT, Chikmagalur

ECE department AIT, Chikmagalur has organised a 5 days Faculty development program on "FPGA implementation on xilinx vivado", with respect to this we are pleased to invite you as a Resource person for this FDP program from 3rd Feb to 7th Feb... Please consider our invitation....we are looking forward positive response from your side

Thanks and best regards

HoD, ECE
AIT, Chikmagalur

Professor & Head
Dept. of Electronics & Communication Engg
Adichunchanagiri Institute of Techn
Chikmagalur - 577 102

Faculty Development Programmme

On

FPGA & Embedded System Design Flow on Zynq using Vivado

3rd to 7th FEB 2020

Organized by,

Department of Electronics and Communication Engineering.

Adichunchanagiri Institute of Technology,

Chikmagalur – 577102

Karnataka. India

www.aitchikmagalur.ac.in

Participating Industry:

ArtiSense Technologies Pvt Ltd, India

About ArtiSense Technologies Pvt Ltd

About the College:

Adichunchanagiri Institute of Technology (AIT) was established in the year 1980 under the auspicious of **Adhichunchanagiri Shikshana Trust(R)** with the blessings of Bhairavaikya **Jagadguru Padmabhushana Sri Sri Sri Dr. Balagangadharanatha Mahaswamiji** to provide technical and other professional education in the rural area of Chikmagalur, the land of Coffee. With the blessings of Jagadguru Sri. Sri. Sri. Nirmalanandanatha Swamiji, AIT is imparting the quality education in Engineering and Management with ethical and spiritual values. The college today has total student strength of about 3200 with 6 branches of Engineering and Technology departments and 3 Master Degree Programmes besides the Management studies. The engineering departments have recognized as research centers under VTU. The college has well equipped laboratory facilities and highly qualified and experienced faculty.

About the Department:

The Department of **Electronics & communication Engineering** came into existence in the year **1981**. The department was under the affiliation of University of Mysore from 1981 to 1992 & under Kuvempu University from 1992 to 1998. Since 1998 the department is under the affiliation of Visvesvaraya Technological University. The PG programme includes M.Tech in Digital Electronics and Communication Systems which offers an experiential learning in advanced topics in engineering. The department is recognized as a research center under VTU and the research scholars from various colleges and industry are participating in active research.

Objectives of the FDP:

A complex Digital system design with constraints has led the embedded system industry to develop ASIC prototyping (FPGA Implementation). In continuation with the evolution of processor technology, researchers have started focusing on many advanced FPGA designs which facilitates more functionality on a single chip. This paradigm shift towards many complex designs has resulted in a renewed interest in use of FPGA to cater the need of various domains such as Image processing, Embedded system design, IoT, and Modern wireless communication systems. Many universities have revised their syllabus in view of industry requirement. This workshop focusing more on hands on session to faculty from various universities and engineering colleges across nation.

Resource Persons:

The resource persons from the industry and academia with the long standing experience will deliver lectures and hands-on training during this course of programme.

Eligibility:

The course is open to the engineering faculty of ECE/TE/EEE/E&I disciplines who are working in Engineering Colleges. Faculty belonging to other disciplines may also apply if this course would supplement their project/research.

Registration:

Free Registration will be based on the first-come-first-serve basis for the maximum of 30 outstation participants.

Important Dates:

Last date for receipt of applications:

Date of intimation regarding selection:

TA and Accommodation:

The lodging and Boarding will be provided in the college campus for the outstation participants based on their request. The TA will be provided as per VTU-VGST norms.

Chief Patron:

Sri. Sri. Sri. Nirmalandanatha Swamiji, pontiff, Adichunchanagiri Maha Samsthana Matt.

Patron:

Sri. Sri. Gunanatha Samiji, Sringeri Shakha Matt.

Organizing Chair:

Dr. C.T Jayadeva, Principal, AIT, Chikmagalur.

Advisors:

Dr. K.E Prakash, Registrar, VTU

Dr. S. Ananth Raj, Consultant, Vision Group on Science and Technology.

Convenor:

Dr. Goutham M.A, Professor and Head, Dept. of Electronics and Communication Engg.,

Coordinator:

Harish Kumar C.R, Asst Professor,

Mahesh D.S Asst Professor

Dept. of Electronics and Communication Engg.,

Address for Communication:

Harish Kumar C.R, Asst Professor,

Mahesh D.S, Asst Professor

Dept. of Electronics and Communication Engg.,

Adichunchanagiri Institute of Technology, Chikmagalur, Karnataka – 577102

Mobile: 9964072122/9964279574

Email:kumar.cr09@gmail.com

Department of Electronics and Communication Engineering,

Faculty Development Programmme

On

FPGA & Embedded System Design Flow on Zynq using Vivado

3rd to 7th FEB 2020

Registration Form

Name: .....

Academic Qualification: .....

Designation: .....

Department:.....

Years of teaching experience: .....

Mobile: .....

E-mail: .....

Address: .....

.....

.....

.....

.....

Do you want accommodation? Yes/No

Place:

Date:

Signature of the Applicant

Dr./Mr./Ms. ----------

---------- is an employee of our organization and is permitted to attend the Faculty Development Programme.

(Signature and Seal of Sponsoring Authority)

(Use the photocopies of the form if required)

Faculty Development Program
on

FPGA & Embedded System Design Flow on Zynq using Vivado

OBJECTIVE OF THE WORKSHOP

A complex Digital system design with constraints has led the embedded system industry to develop ASIC prototyping (FPGA Implementation). In continuation with the evolution of processor technology, researchers have started focusing on many advanced FPGA designs which facilitates more functionality on a single chip. This paradigm shift towards many complex designs has resulted in a renewed interest in use of FPGA to cater the need of various domains such as Image processing, Embedded system design, IoT, and Modern wireless communication systems. Many universities have revised their syllabus in view of industry requirement. This workshop focusing more on hands on session to faculty from various universities and engineering colleges across nation.

WORKSHOP AGENDA

Day 1:

- 7-Series Architecture Overview
- Vivado Design Flow
  - Use Vivado IDE to create a simple HDL design. Simulate the design using the XSIM HDL simulator available in Vivado design suite. Generate the bitstream and verify in hardware.
- Synthesis Technique
- Synthesizing a RTL Design
  - Synthesize a design with the default settings as well as other settings changed and observe the effect.

Day 2:

- Implementation and Static Timing Analysis
- Implementing the Design
  - Implement the synthesized design of previous lab, perform timing analysis, generate bitstream, download the bitstream and verify the functionality.

Demonstration of Image processing Using ZedBoard

Day 3:

- Introduction to Embedded System Design using Zynq
- Simple Hardware Design

- Create a Vivado project and use IP Integrator to develop a basic embedded system for a target board.

Day 4:

- **Zynq Architecture**
- Extending the Embedded System into Programmable Logic
- Adding Peripherals in Programmable Logic
  - Extend the hardware system by adding AXI peripherals from the IP catalog.
- Adding Your Own IP Peripheral
- Creating and Adding Your Own Custom IP
  - Use the Manage IP feature of Vivado to create a custom IP and extend the system with the custom peripheral.

Day 5:

- **Software Development and Debugging**
- Software Debugging Using SDK
  - Use API to drive CPU's timer. Perform software debugging using SDK.

Demonstration of signal processing (XADC) Using Artix FPGA Board

Cost of the programme:
Rs.3000/- per faculty member

Number of Resource persons: 03
Technical Assistance Team : 03

Name: **Vijendra V**
Designation: **Application Engineer**

Professional Experience: 3.5 Years
Bangalore 560034

Technical experience areas:

Programming Languages: VHDL, Verilog, Embedded C/C++
Operating System: Windows & Linux

FPGA Tools: Vivado Design Suite which includes IP Integrator, Vivado Simulator, Vivado Logic Analyzer, Vivado HLS and Vivado System Generator.

ASIC Tools: Mentor Graphics Front end and Backend Design Tools includes HDL Designer, Precision, Leonardo Spectrum, Questasim, Pyxis schematic and Layout, Calibre.

As a Technical resource person handled various workshops across INDIA. The topics include the following:

- FPGA Design flow using Xilinx Vivado Design Suite
- Embedded System Design using Xilinx Vivado Design suite on Zynq-7000 Soc.
- DSP Design on FPGA using Xilinx Vivado System Generator
- System Design flow using Xilinx SDSoC Tools.
- ASIC Design using Mentor Graphics EDA Design Tools.
- DFT using Tessent FastScan, ATPG, BIST.

Professional Qualification:

Part Time Ph.d (Research Scholar) Pursuing at Center for PG Studies, Visvesvaraya Technological University, Belagavi, Visvesvaraya Technological University, Belagavi-Karnataka, India.

Papers Publications:

1. **Vijendra V, Meghana Kulkarni and Rajesh Murgan** "ECG Pattern Recognition and Beat Classification using Internet of Things and Hardware Acceleration on ZynQ (SOC) Platform with High Performance Computational PCIe Protocol Published in BIODEVICES - 12th International Conference on Biomedical Electronics and Devices conference at Prague, Czech Republic, Europe - February 22-24, 2019, pages 261-268 with SCITPRESS Digital Library, Springer Proceedings, dblp library Germany- **ISBN: 978-989-758-353-7.**
2. **Vijendra and Meghana Kulkarni,** "ECG Pattern Recognition and Optimized Deep Learning Algorithms using Machine Learning techniques : An Illustrative Survey" Published in IEEE

Digital Xplore - IEEE 4th International Conference for Convergence in Technology , IC4 conference at Mangalore, 27-28th October 2018.

3. **Vijendra and Meghana Kulkarni,** " Automatic ECG Signals Recognition Based on Time Domain Features Extraction Using Fiducial Mean Square Algorithm" Springer Publications in Computational Intelligence: Theories, Applications and Future Directions - Volume I, Pages 18-94. Advances in Intelligent Systems and Computing book series (AISC, volume 798). **ISBN 978-981-13-1131-4, © Springer Nature Singapore Pte Ltd. 2019**

4. **Vijendra V and Meghana Kulkarni,** "ECG signal filtering using DWT Haar Wavelets coefficient techniques", Proceedings of the 1st International Conference on Emerging Trends in Engineering, Technology and Science, Published in IEEE digital Explore library with **ISBN:978-1-4673-6725-7**, KCE, Punalkulam, Thanjavur, Tamilnadu, INDIA, February 24-26, 2016 pp. 382-387.

5. **Vijendra V and Meghana Kulkarni,** "Fuzzy controlled ID Interpretation based Diagnostics systems", International Conference on Health and Technical Research(ICHTR) at Manipal institute of Technology(MIT) Dec 22-24th 2015,Udupi, Karnataka, INDIA. Peer review and publications in SCOPUS Indexed **[American science Publishers - Volume 23, Number 3]**

Papers Presentations:

- Fabrication of a PLDC Cell using Near Infrared OLED Published in International Journal of Inventive Engineering and Sciences (IJIES) ISSN: 2319–9598, Volume-3 Issue-2, January 2015.
- Published in IEEE Xpolre under the titled Design and implementation of GSM/EDGE based 2.5G Polar transmitter at IEEE international Conference in collaboration with Rathinam Technical campus at Coimbatore, Tamilnadu, India.
- National level paper presentation on Integer wavelet based secret data hiding in M.V. Jayraman College at Bangalore.
- Participated in BTI College of Engineering for E3 National Conference at Bangalore.
- Participated in National level conferences on Design and Implementation of phase modulation for polar transmitter and paper presentation at Kollapur, Maharastra.

|| Jai Sri Gurudev ||
Sri AdichunchanagiriShikshana Trust®

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Chikkamagaluru - 577 102, Karnataka, India

DEPARTMENT OF ELETRONICS AND COMMUNICATION ENGINEERING Organizes

FIVE DAYS FACULTY DEVELOPMENT PROGRAMME

ON

"FPGA & Embedded system design flow on Zynq using Vivado"

03-02-2020 To 07-02-2020

Registration Details

Sl. No	Participant Name	College/ Department	Mail Id	Mobile No	Signature
1.	Dr.M.A.Goutham	AIT / ECE	magoutham@gmail.com	9448554971	
2.	Dr A.P.JagdishChandra	AIT / ECE	apjchandra@gmail.com	9448759176	
3.	M.Suguna	AIT/ECE	Suguna.agu15@gmail.com	8762935787	
4.	H.R.vani	AIT/ECE	vani4ait@gmail.com	9448692323	
5.	H.K.chandrashekar	AIT/ECE	hkchandrashekar@gmail.com	9448640078	
6.	Dr. Kumuda T.	AIT/E&C	kumuda.thmmeiaah@gmail.com	9448759132	
7.	Dr.Harish M.S.	AIT/E&C.	harishmtech2003@yahoo.com	9740333412	
8.	Dr.Anil Kumar C.	ECE	Onlyoneanil@gmail.com	9902037956	
9.	Suma M.	ECE	suma.aug13@gmail.com	9481653956	
10.	MadhuprakashR	ECE	Madhuprakash@gmail.com	7795361426	

11.	Bharath	ECE	bharathkote7@gmail.com	9900792744	
12.	Mahesh D S	ECE	Maheshsbr2@gmail.com	9964279574	
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19.	Harish kumar C R	ECE	kumar.cr09@gmail.com	9964072182	
20.	Rathan H D	ECE	rathanhadoni@gmail.com	9481579801	
21.	Pallavi C S	ECE	Pallavisadananda@gmail.com	9964843232	
22.	Anitha K.T.	ECE	anitha.darshini24@gmail.com	9686749857	
23.	Joysun D Souza	~~ECE~~ E&E	joysun.dsouza@gmail.com	8105184858	
24.	Poshitha B	E&E	Poshitha_24@yahoo.com	8951109478	

Signature of the Coordinator's

Signature of the HOD

Professor & Head
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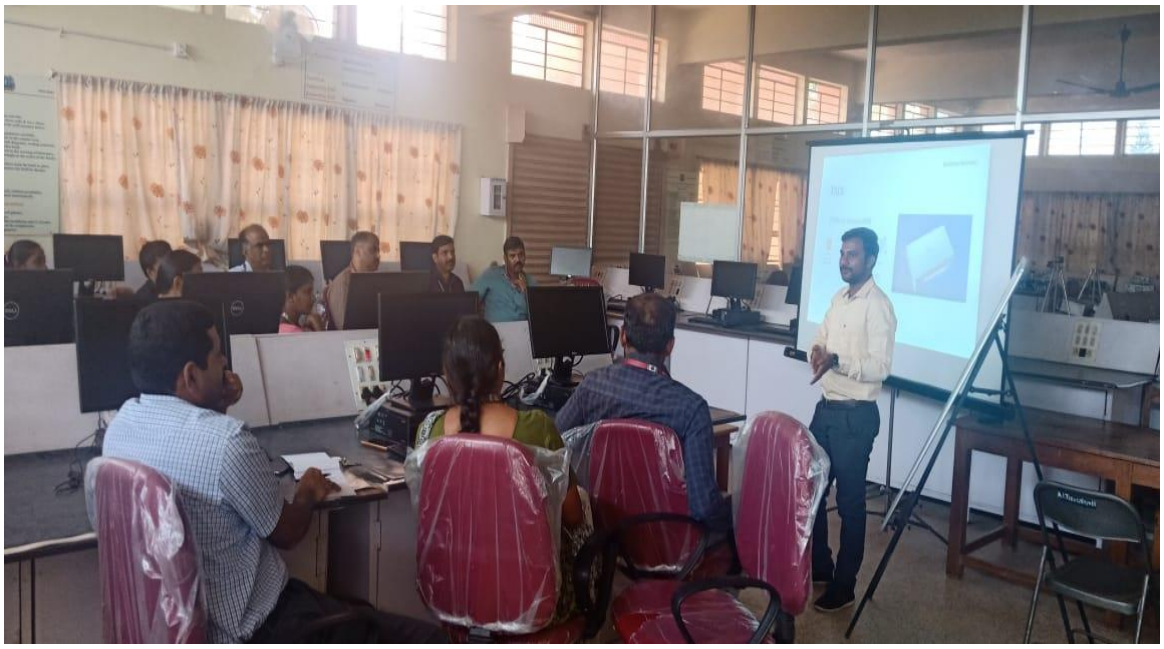
Adichunchanagiri Institute of Technology
Chikmagalur - 577 102

Department of Electronics and Communication Engineering

Faculty Development Program

Five days Faculty development program on FPGA and Embedded design flow on ZYNQ using vivado was conducted by EC department from 03.02.2020 to 07-02-2020. In association with ArtiSense Technologies Pvt. Ltd. Dr. Shashidara K.S, Professor, ECE Dept., NMIT, Sujeeth Kumar, Application Engineer and Vijendra V, Application Engineer, were the resource persons for FDP.



Dr. Shashidara K.S and Faculties during FDP

ADICHUNCHANAGIRI INSTITUTE OF TECHNOLOGY

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Department of Electronics and Communication Engineering

FDP on FPGA & Embedded System Design Flow on Zynq using Vivado

Attendance Sheet

Sl. No.	Name of the Candidates	3/2/2020	4/2/2020	5/2/2020	6/2/2020	7/2/2020
1	Dr.M.A.Goutham					
2	Dr. A.P.Jagdeesh Chandra					
3	M. Suguna					
4	H.R.Vani					
5	H.K.Chandrashekar					
6	Dr. Kumuda T.					
7	Dr.M.S.Harish					
8	Anil Kumar C.					
9	M.Suma					
10	Madhu Prakash R.					
11	Bharath					
12	Mahesh D.S.					
13	Usha K.P.					
14	Manjula U.R..					
15	Nagaveni C.R					
16	Chandrakala C.T.					
17	Bhavya A					
18	Divya G S					
19	Harish Kumar C.R.					
20	Rathan H D					
21	Pallavi C S					
22	Anitha K T					
23	Joysun D Souza					
24	Poshitha B					

Coordinator

Head of the Department

Professor & Head
Dept. of Electronics & Communication Eng
Adichunchanagiri Institute of Technology
Chikmagalur - 577 102