ವಿಶ್ವೇಶ್ವರಯ್ಯ ತಾಂತ್ರಿಕ ವಿಶ್ವವಿದ್ಯಾಲಯ
ಬೆಳಗಾವಿ ಅಥವಾ ಗುಲ್ಬರ್ಗಾ ಜಿಲ್ಲೆಗಳ ಪ್ರದೇಶಗಳನ್ನು ಒಳಗೊಂಡಂತೆ ಕರ್ನಾಟಕ ಸರ್ಕಾರದಿಂದ ಸ್ಥಾಪಿತವಾದ ರಾಜ್ಯ ವಿಶ್ವವಿದ್ಯಾನಿಲಯ
"ಜ್ಞಾನ ಸಂಗಮ", ಬೆಳಗಾವಿ-೫೯೦೦೧೮, ಕರ್ನಾಟಕ, ಭಾರತ

Visvesvaraya Technological University
(State University of Government of Karnataka Established as per the VTU Act, 1994)
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Phone: (0831) 2498100
Fax: (0831) 2405467

Registrar

Ref: VTU/BGM/BOS/A9/2020-21 /6652 Date: 12 MAR 2021

Revised -NOTIFICATION

Subject: Academic Calendar for I semester (revised) B.E./B.Tech./B.Plan./B.Arch., for the year 2020-21 regarding...

Reference:

1. VTU/BGM/SO2/2020-21/5296, dated 15.01.2021
2. Hon'ble Vice-Chancellor's approval dated 12.03.2021

Revised Academic Calendar for I semester of B.E./B.Tech./B.Arch./B.Plan., for the Year 2020-21 is hereby notified as below-

Events	Dates
Commencement of ODD Semester	14.12.2020
Last Working day of ODD Semester	**10.04.2021**
Practical Examinations	**05.05.2021 to 15.05.2021**
Theory Examinations	**19.04.2021 to 03.05.2021**
Internship	-----
Internship Viva-Voce	-----
Professional training / Organization study	-----
Commencement of EVEN Semester	**19.05.2021**

The Principals of Affiliated, Constituent, and Autonomous Engineering Colleges are hereby informed to bring the contents of this Notification to the notice of all the concerned.

Sd/-
REGISTRAR

To,

1. The Principals of all affiliated/ constituent /Autonomous Engineering Colleges under the ambit of VTU Belagavi.
2. The Chairpersons of all Departments, Centres for PG Studies in Belagavi, Kalaburgi, Muddenahalli, and Mysore.

Copy to.

1. To the Hon'ble Vice-Chancellor through the secretary to VC, VTU Belagavi for information
2. The Registrar (Evaluation), VTU Belagavi for information.
3. The Regional Directors (I/c) of all the regional offices of VTU for circulation.
4. The Special Officer CNC VTU Belagavi for uploading on VTU website
5. PS to Registrar VTU Belagavi
6. All the concerned Special Officer/s and Caseworker/s of the academic section, VTU, Belagavi

Ranjan C.B.
REGISTRAR 12/03/21

1/1

Professor & Head
Dept. of Electronics & Communication Engg
Adichunchanagiri Institute of Technology,
Chikmagalur - 577 102

ವಿಶ್ವೇಶ್ವರಯ್ಯ ತಾಂತ್ರಿಕ ವಿಶ್ವವಿದ್ಯಾಲಯ
ಕರ್ನಾಟಕ ಸರ್ಕಾರದ ಅಧಿನಿಯಮ ೧೯೯೪ರ ಅಡಿಯಲ್ಲಿ ಕರ್ನಾಟಕ ರಾಜ್ಯಪತ್ರದಲ್ಲಿ ಪ್ರಕಟವಾದ ರಾಜ್ಯ ವಿಶ್ವವಿದ್ಯಾಲಯ
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Registrar

Phone: (0831) 2498100
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Ref: VTU/BGM/BOS/A9/2020-21/948

Date: 15 APR 2021

CIRCULAR

Subject: Commencement of EVEN semesters of UG programs for the year 2020-21 regarding...

Reference: Hon'ble Vice-Chancellor Approval dated 15.04.2021

Concerning the subject cited above, the commencement of EVEN semesters of B.E./B.Tech./B.Plan./B.Arch. programs of University will be from **19th April 2021**. The academic calendar related to the EVEN semester/s is notified as attached.

The Principals of Affiliated, Constituent, and Autonomous Engineering Colleges are hereby informed to bring the contents of this circular to the notice of all the concerned.

Sd/-
REGISTRAR

Encl: As mentioned above.

To,

1. The Principals of all affiliated/ constituent /Autonomous Engineering Colleges under the ambit of VTU Belagavi.
2. The Chairpersons of all Departments, Centres for PG Studies in Belagavi, Kalaburgi, Muddenahalli, and Mysore.

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5. PS to Registrar VTU Belagavi
6. All the concerned Special Officer/s and Caseworker/s of the academic section, VTU, Belagavi

15.4.2021
REGISTRAR

Professor & Head
Dept. of Electronics & Communication Engg
Adichunchanagiri Institute of Technology,
Chikmagalur - 577 102

ವಿಶ್ವೇಶ್ವರಯ್ಯ ತಾಂತ್ರಿಕ ವಿಶ್ವವಿದ್ಯಾಲಯ
"ಶಿಟಿಯು ಅಧಿನಿಯಮ ೧೯೯೪"ರ ಅಡಿಯಲ್ಲಿ ಕರ್ನಾಟಕ ಸರ್ಕಾರದಿಂದ ಸ್ಥಾಪಿತವಾದ ರಾಜ್ಯ ವಿಶ್ವವಿದ್ಯಾಲಯ
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Ref: VTU/BOS/A9/2020-21 / 2702

Date: 22 SEP 2021

NOTIFICATION

Subject: Commencement of ODD semester of UG-PG programs for the year 2021-22 regarding...

Reference: Hon'ble Vice-Chancellor's Approval dated: 22.09.2022

The academic calendar concerned to ODD semesters of Under-graduate and Post-graduate, programmes of University is hereby notified as below-.

The Principals of Affiliated, Constituent, and Autonomous Engineering Colleges are hereby informed to bring the content of this circular to the notice of all the concerned.

Sd/-
REGISTRAR

Encl: As mentioned above.

To,

1. The Principals of all affiliated/ constituent /Autonomous Engineering Colleges under the ambit of VTU Belagavi.
2. The Chairpersons of all Departments, Centres for PG Studies in Belagavi, Kalaburgi, Muddenahalli, and Mysore.

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4. The Special Officer CNC VTU Belagavi for uploading on VTU website
5. PS to Registrar VTU Belagavi
6. All the concerned Special Officer/s and Caseworker/s of the academic section, VTU, Belagavi

REGISTRAR

VBY 5/10/21

Professor & Head
Dept. of Electronics & Communication Engg
Adichunchanagiri Institute of Technology,
Chikmagalur - 577 102

ವಿಶ್ವೇಶ್ವರಯ್ಯ ತಾಂತ್ರಿಕ ವಿಶ್ವವಿದ್ಯಾಲಯ
"ವಿದ್ಯಯು ಅಧಿಸಮಮ ಗ್ರಂಥಗಳ ಅಧ್ಯಯನ ಕರ್ನಾಟಕ ರಾಜ್ಯದಲ್ಲಿ ತಾಂತ್ರಿಕ ಶಿಕ್ಷಣವನ್ನು ಪ್ರಸಾರಗೊಳಿಸಲು
"ಜ್ಞಾನ ಸಂಗಮ", ಬೆಳಗಾವಿ-೫೯೦೦೧೮, ಕರ್ನಾಟಕ, ಭಾರತ
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Dr. A. S. Deshpande B.E., M.Tech., Ph.D.
Registrar

Phone: (0831) 2498100
Fax: (0831) 2405467

Ref: VTU/BOS/SO2/2020-21/5082

Date: 10 JAN 2022

NOTIFICATION

Subject: Revised-Academic Calendar of III semester B.E./B.Tech. programs for AY 2021-22 regarding...

Reference: EC resolution no. 2.1.4, dated: 04.01.2022

The academic calendar concerned to 3rd semester of B.E. / B.Tech. Programs of University is hereby re-notified as below-

Revised-Academic Calendar for 3rd Semester of B.E./B.Tech. Programs for AY 2021-22

Events	Existing Dates	Revised Dates
Commencement of ODD Semester	18.10.2021	18.10.2021
Last Working day of ODD Semester	19.02.2022	25.03.2022
Practical Examination For regular students	21.02.2022 To 04.03.2022	28.03.2022 To 31.03.2022
Theory Examinations For both regular and lateral entry students	07.03.2022 To 25.03.2022	01.04.2022 To 20.04.2022
Practical Examination For Lateral Entry students		21.04.2022 To 26.04.2022
Commencement of EVEN Semester	11.04.2022	02.05.2022

- The college has to conduct the separate classes for the lateral entry students
- Readmitted students, Change of College opted students and change of Branch opted students may be permitted to appear for the classes along with lateral entry students for syllabus coverage.

Professor & Head
Dept. of Electronics & Communication Engg
Adichunchanagiri Institute of Technology,
Chikmagalur - 577 102

- The Institute needs to function for **six days** a week with additional hours (Saturday **is a full working day).** #if required the college can plan to have extra classes even on Sundays also.
- If any of the above dates are declared to be a holiday then the corresponding event will come into effect on the next working day.
- Notification regarding the Calendar of Events relating to the conduct of University **Examinations** will be issued by the Registrar (Evaluation) from time to time.
- Academic Calendar **may be modified** based on guidelines/directions issued in the future by MHRD/UGC/AICTE/State Government.
- Academic Calendar is also applicable for **Autonomous Colleges.** In case if any changes are to be effected by Autonomous Colleges in the academic terms and examination schedule, they could do so with the approval of the University.
- The faculty/staff shall be available to undertake any work assigned by the university.
- The college has to conduct offline classes to cover 80% of the syllabus of the courses, however, 20% of the syllabus can be covered in virtual (Online) mode.
- Attendance of the student's offline/online classes is mandatory and record should be maintained and submitted to university whenever informed.

The Principals of Affiliated, Constituent, and Autonomous Engineering Colleges are hereby informed to bring the content of this circular to the notice of all the concerned.

Sd/-
REGISTRAR

Encl: As mentioned above.

To,

1. The Principals of all affiliated/ constituent /Autonomous Engineering Colleges under the ambit of VTU Belagavi.

Copy to.

1. To the Hon'ble Vice-Chancellor through the secretary to VC, VTU Belagavi for information
2. The Registrar (Evaluation), VTU Belagavi for information.
3. The Regional Directors (I/c) of all the regional offices of VTU for circulation.
4. The Director SMUITI CNC, VTU Belagavi request touploadAcademic Calendar on the VTU web portal
5. PS to Registrar VTU Belagavi
6. All the concerned Special Officer/s and Caseworker/s of the academic section, VTU, Belagavi

REGISTRAR

Professor & Head
Dept. of Electronics & Communication Engg
Adichunchanagiri Institute of Technology
Chikmagalur - 577 102

ವಿಶ್ವೇಶ್ವರಯ್ಯ ತಾಂತ್ರಿಕ ವಿಶ್ವವಿದ್ಯಾಲಯ
"ಬೆಳಗಾವಿಯ ಅಧಿನಿಯಮ ರಾಷ್ಟ್ರೀಯ ಅಡಿಯಲ್ಲಿ ಕರ್ನಾಟಕ ಸರ್ಕಾರದಿಂದ ಸ್ಥಾಪಿತವಾದ ರಾಜ್ಯ ವಿಶ್ವವಿದ್ಯಾಲಯ"
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Phone: (0831) 2498100
Fax: (0831) 2405467

Registrar

Ref: VTU/BOS/SO2/2020-21 / 6335 Date: 15 MAR 2022

Revised – NOTIFICATION (1)

Subject: Revised-Academic Calendar of I semester B.E./B.Tech./B.Plan./B.Arch., and III semesters B.E./B.Tech. programs for AY 2021-22 regarding...

Reference: Hon'ble Vice-Chancellor's approval dated: 14.03.2022

The academic calendar concerned to I semester B.E./B.Tech./B.Plan./B.Arch and III semester of B.E. / B.Tech.Programs of University is hereby re-notified as below-

Events	I semester B.E./B.Tech./	I semester B.Plan./B.Arch.	III semester B.E./B.Tech.
Commencement of ODD Semester	13.12.2021	13.12.2021	18.10.2021
Last Working day of ODD Semester	13.04.2022	13.04.2022	13.04.2022
Practical Examinations	18.04.2022 to 27.04.2022	18.04.2022 to 27.04.2022	16.04.2022 to 23.04.2022
Theory Examinations	28.04.2022 to 20.05.2022	28.04.2022 to 20.05.2022	25.04.2022 to 15.05.2022
Commencement of EVEN Semester	23.05.2022	23.05.2022	16.05.2022

- If any of the above dates are declared to be a holiday, then the corresponding event will come into effect on the next working day.
- Notification regarding the Calendar of Events relating to the conduct of University Examinations will be issued by the Registrar (Evaluation) from time to time.
- Academic Calendar may be modified based on guidelines/directions issued in the future by MHRD/UGC/AICTE/State Government.
- Academic Calendar is also applicable for Autonomous Colleges. In case if any changes are to be effected by Autonomous Colleges in the academic terms and examination schedule, they could do so with the approval of the University.
- The faculty/staff shall be available to undertake any work assigned by the university.

The Principals of Affiliated, Constituent and Autonomous Engineering Colleges are hereby informed to bring the content of this circular to the notice of all the concerned.

Sd/-
REGISTRAR

To,

1. The Principals of all affiliated/ constituent /Autonomous Engineering Colleges under the ambit of VTU Belagavi..

Professor & Head
Dept. of Electronics & Communication Engg
Adichunchanagiri Institute of Technology.
Chikmagalur - 577 102

ವಿಶ್ವೇಶ್ವರಯ್ಯ ತಾಂತ್ರಿಕ ವಿಶ್ವವಿದ್ಯಾಲಯ
"ವಿಟಿಯು ಅಧಿನಿಯಮ ೧೯೮೬ರ ಅಡಿಯಲ್ಲಿ ಕರ್ನಾಟಕ ಸರ್ಕಾರದಿಂದ ಸ್ಥಾಪಿತವಾದ ರಾಜ್ಯ ವಿಶ್ವವಿದ್ಯಾಲಯ
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Dr. A. S. Deshpande B.E., M.Tech., Ph.D.
Registrar

Phone: (0831) 2498100
Fax: (0831) 2405467

Ref: VTU/BGM/BOS/A9/2021-22 6521

Date: 30 MAR 2022

Revised-NOTIFICATION

Subject: -Academic Calendar of EVEN semesters of UG & PG programs of University regarding...

Reference: Hon'ble Vice-Chancellor's approval dated: 25.03.2022

The academic calendar concerned to IV semesters of B.Plan/B.Arch., VI/VIII semesters of B.E./B.Tech./B.Plan/B.Arch., IV semesters of MCA/M.Arch/M.Tech., and VI semester of MCA(2018 scheme), Programs of University is hereby notified in enclosed sheet;

The Principals of Affiliated, Constituent, and Autonomous Engineering Colleges are hereby informed to bring the content of this circular to the notice of all concerned.

Sd/-
REGISTRAR

To,

1. The Principals of all affiliated/ constituent /Autonomous Engineering Colleges under the ambit of VTU Belagavi.

Copy to.

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2. The Registrar (Evaluation), VTU Belagavi for information.
3. The Regional Directors (I/c) of all the regional offices of VTU for circulation.
4. The Director SMU ITI CNC, VTU Belagavi requested to make arrangements to upload Academic Calendar on the VTU web portal
5. PS to Registrar VTU Belagavi
6. All the concerned Special Officer/s and Caseworker/s of the academic section, VTU, Belagavi

REGISTRAR

Professor & Head
Dept. of Electronics & Communication Engg
Adichunchanagiri Institute of Technology
Chikmagalur - 577 102

1/1

ವಿಶ್ವೇಶ್ವರಯ್ಯ ತಾಂತ್ರಿಕ ವಿಶ್ವವಿದ್ಯಾಲಯ
(ವಿತಾಯುಅಧಿನಿಯಮ್ ೧೯೮೬ರಅಡಿಯಲ್ಲಿಕರ್ನಾಟಕಸರ್ಕಾರದಿಂದಸ್ಥಾಪಿತವಾದರಾಜ್ಯವಿಶ್ವವಿದ್ಯಾಲಯ)ಜ್ಞಾನ
ಸಂಗಮ, ಮಚ್ಛೆ, ಬೆಳಗಾವಿ-೫೯೦೦೧೮
Visvesvaraya Technological University
(The State University of Govt. Karnataka, Established as per VTU Act 1994)
"JnanaSangama" Machhe, Belagavi-590018, www.vtu.ac.in

Dr. A. S. Deshpande B.E., Tech., Ph.D.
Registrar

Phone: (0831) 2498100
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Ref. No. VTU/BGM/BOS/2021-22/ 149 Date: 19 APR 2022

Revised-NOTIFICATION

Subject: -Revised Academic Calendar of I semester B.E./B.Tech./B.Plan./B.Arch. programs of University regarding...

Reference: Hon'ble Vice-Chancellor's approval dated: 08.04.2022

The revised academic calendar concerned I semester **B.E./B.Tech./B.Plan./B.Arch.** programsof University are hereby notified as below-

	Existing dates	Revised dates
Commencementof ODDSemester	13.12.2021	13.12.2021
Last Workingday of the ODDSemester	13.04.2022	30.04.2022
Practical Examination	18.04.2022 To 27.04.2022	02.05.2022 To 10.05.2022
Theory Examinations	28.04.2022 To 20.05.2022	12.05.2022 To 30.05.2022
Commencementof EVEN Semester	23.05.2022	01.06.2022

The Principals of Affiliated, Constituent and Autonomous Engineering Colleges are hereby informed to bring the content of this circular to the notice of all concerned.

Sd/-
REGISTRAR

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Professor & Head
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Adichunchanagiri Institute of Technology,
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ಎಂತಾಯುಳಧಿನಿಯಮ೧೯೯೪ರಅಡಿಯಲ್ಲಿಕರ್ನಾಟಕಸರ್ಕಾರದಿಂದಸ್ಥಾಪಿತವಾದರಾಜ್ಯವಿಶ್ವವಿದ್ಯಾಲಯ'ಜ್ಞಾನ
ಸಂಗಮ' ಮಚ್ಛೆ, ಬೆಳಗಾವಿ-590018
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Dr. A. S. Deshpande B.E., Tech., Ph.D.
Registrar

Phone: (0831) 2498100
Fax: (0831) 2405467

Ref. No. VTU/BGM/BOS/2021-22/ 149

Date: 19 APR 2022

Revised-NOTIFICATION

Subject: -Revised Academic Calendar of I semester B.E./B.Tech./B.Plan./B.Arch. programs of University regarding...

Reference: Hon'ble Vice-Chancellor's approval dated: 08.04.2022

The revised academic calendar concerned I semester **B.E./B.Tech./B.Plan./B.Arch.** programsof University are hereby notified as below-

	Existing dates	Revised dates
Commencementof ODDSemester	13.12.2021	13.12.2021
Last Workingday of the ODDSemester	13.04.2022	30.04.2022
Practical Examination	18.04.2022 To 27.04.2022	02.05.2022 To 10.05.2022
Theory Examinations	28.04.2022 To 20.05.2022	12.05.2022 To 30.05.2022
Commencementof EVEN Semester	23.05.2022	01.06.2022

The Principals of Affiliated, Constituent and Autonomous Engineering Colleges are hereby informed to bring the content of this circular to the notice of all concerned.

Sd/-
REGISTRAR

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ವಿತಾಯುಅಧಿನಿಯಮ್೧೯೯೪ರಅಡಿಯಲ್ಲಿಕರ್ನಾಟಕಸರ್ಕಾರದಿಂದಸ್ಥಾಪಿತವಾದರಾಜ್ಯವಿಶ್ವವಿದ್ಯಾಲಯ'ಜ್ಞಾನ
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Dr. A. S. Deshpande B.E., Tech., Ph.D.
Registrar

Phone: (0831) 2498100
Fax: (0831) 2405467

Ref. No. VTU/BGM/BOS/2021-22/ 709 Date: 29 APR 2022.

NOTIFICATION

Subject: Academic Calendar of IV semester MBA, II semester B.Sc., IV semester B.E./ B.Tech., and (revised) VI semester B.E./B.Tech./B. Plan and (revised) I semester B.E./B.Tech./B.Plan/B.Arch. programs of University regarding...

Reference Hon'ble Vice-Chancellor's approval dated: 25.04.2022

Academic Calendar of IV semester MBA, II semester B.Sc., IV semester B.E./ B.Tech., **(revised)** VI semester B.E./B.Tech./B.Plan., and **(revised)** I semester B.E./B.Tech./ B.Plan./ B.Arch., programs of the University are shown on the 2nd page of this notification.

The Principals of Affiliated, Constituent and Autonomous Engineering Colleges are hereby informed to bring the academic calendar to the notice of all concerned.

Sd/-
REGISTRAR

To,

1. The Principals of all affiliated/ constituent /Autonomous Engineering Colleges under the ambit of VTU Belagavi.
2. The chairperson, Department of Mechanical Engineering /Civil Engineering /Computer Science and Engineering and Business Studies of the University.

Copy to.

1. To the Hon'ble Vice-Chancellor through the secretary to VC, VTU Belagavi for information
2. The Registrar (Evaluation), VTU Belagavi for information.
3. The Regional Directors (I/c) of all the regional offices of VTU for circulation.
4. The Director SMUITI, VTU Belagavi for information and to make arrangements to upload Academic Calendar on the VTU web portal.
5. The Director of Physical Education, VTU Belagavi for information
6. PS to Registrar VTU Belagavi
7. All the concerned Special Officer/s and Caseworker/s of the academic section, VTU, Belagavi

Sd/-
REGISTRAR

Professor & Head
Dept. of Electronics & Communication Engg
Adichunchanagiri Institute of Technology
Chikmagalur - 577

ವಿಶ್ವೇಶ್ವರಯ್ಯ ತಾಂತ್ರಿಕ ವಿಶ್ವವಿದ್ಯಾಲಯ
ವಿತಾಯುಲಧಿನಿಯಮ್೧೯೯೪ರಅಡಿಯಲ್ಲಿಕರ್ನಾಟಕಸರ್ಕಾರದಿಂದಸ್ಥಾಪಿತವಾದರಾಜ್ಯವಿಶ್ವವಿದ್ಯಾಲಯ"ಜ್ಞಾನ
ಸಂಗಮ" ಮಚ್ಛೆ, ಬೆಳಗಾವಿ-590018
Visvesvaraya Technological University
(The State University of Govt. Karnataka, Established as per VTU Act 1994)
"JnanaSangama" Machhe, Belagavi-590018, www.vtu.ac.in

Dr. A. S. Deshpande B.E., Tech., Ph.D.
Registrar

Phone: (0831) 2498100
Fax: (0831) 2405467

Ref. No. VTU/BGM/BOS/2021-22/ 709 Date: 29 APR 2022.

NOTIFICATION

Subject: Academic Calendar of IV semester MBA, II semester B.Sc., IV semester B.E./ B.Tech., and (revised) VI semester B.E./B.Tech./B. Plan and (revised) I semester B.E./B.Tech./B.Plan/B.Arch. programs of University regarding...

Reference Hon'ble Vice-Chancellor's approval dated: 25.04.2022

Academic Calendar of IV semester MBA, II semester B.Sc., IV semester B.E./ B.Tech., **(revised)** VI semester B.E./B.Tech./B.Plan., and **(revised)** I semester B.E./B.Tech./ B.Plan./ B.Arch., programs of the University are shown on the 2nd page of this notification.

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Sd/-
REGISTRAR

Professor & Head
Dept. of Electronics & Communication Engg
Adichunchanagiri Institute of Technology
Chikmagalur - 577

ವಿಶ್ವೇಶ್ವರಯ್ಯ ತಾಂತ್ರಿಕ ವಿಶ್ವವಿದ್ಯಾಲಯ

ವಿತಾಯು ಅಧಿನಿಯಮ್ ೧೯೯೪ರ ಅಡಿಯಲ್ಲಿ ಕರ್ನಾಟಕ ಸರ್ಕಾರದಿಂದ ಸ್ಥಾಪಿತವಾದ ರಾಜ್ಯ ವಿಶ್ವವಿದ್ಯಾಲಯ

"ಜ್ಞಾನ ಸಂಗಮ" ಮಚ್ಛೆ, ಬೆಳಗಾವಿ-590018

Visvesvaraya Technological University

(The State University of Govt. Karnataka, Established as per VTU Act 1994)

"JnanaSangama" Machhe, Belagavi-590018, www.vtu.ac.in

Dr. A. S. Deshpande B.E., Tech., Ph.D.
Registrar

Phone: (0831) 2498100
Fax: (0831) 2405467

Ref. No. VTU/BGM/BOS/2021-22/ 834 Date: 10 MAY 2022

Revised-NOTIFICATION

Subject: - Revised Academic Calendar of IV semester B.E./B.Tech., programs of University regarding...

Reference:

1. Hon'ble Vice-Chancellor's approval dated: 05.05.2022
2. VTU/BGM/BOS/2021-22/709, dated 29.04.2022
3. VTU/Exam/2022-2023110, dated 01.05.2022
4. VTU/Exam/QPDS/2022-23/114, dated 01.05.2022

The revised academic calendar concerned **IV semester B.E./B.Tech.,** programs of University are hereby notified as below-

Events	Existing dates	Revised Dates
Commencement of EVEN Semester	16.05.2022	**23.05.2022**
Last Working day of the EVEN Semester	27.08.2022	**03.09.2022**
Practical/Viva Examination	01.09.2022 To 08.09.2022	**05.09.2022 To 13.09.2022**
Theory Examinations	12.09.2022 To 30.09.2022	**16.09.2022 To 08.10.2022**
Commencement of next ODD Semester	10.10.2022	**10.10.2022**

The Principals of Affiliated, Constituent and Autonomous Engineering Colleges are hereby informed to bring the academic calendar to the notice of all concerned.

Sd/-
REGISTRAR

To,

1. The Principals of all affiliated/ constituent /Autonomous Engineering Colleges under the ambit of VTU Belagavi.
2. The chairperson, Department of Mechanical Engineering /Civil Engineering /Computer Science and Engineering and Business Studies of the University.

Professor & Head
Dept. of Electronics & Communication Engg
Adichunchanagiri Institute of Technology.
Chikmagalur - 577 102

Copy to.

1. To the Hon'ble Vice-Chancellor through the secretary to VC, VTU Belagavi for infor
2. The Registrar (Evaluation), VTU Belagavi for information.
3. The Regional Directors (I/c) of all the regional offices of VTU for circulation.
4. The Director I/c. ITISMU, VTU Belagavi for information and to make arrangements upload Academic Calendar on the VTU web portal.
5. The Director of Physical Education, VTU Belagavi for information
6. PS to Registrar VTU Belagavi
7. All the concerned Special Officer/s and Caseworker/s of the academic section, VTU Belagavi

REG

Professor & Head
Dept. of Electronics & Communication Engg
Adichunchanagiri Institute of Technology,
Chikmagalur - 577 102

Academic Calendar for IV sem MBA / IV semB.E./B.Tech.(**Revised**) VI sem B.E./B.Tech /B.Plan., (**Revised**) B.E./B.Tech./B.Arch./B.Plan., and II sem B.Sc. Programs for AY-2021-22

	VI semester B.E./B.Tech. (Revised)	VI semester B.Plan. (Revised)	IV Semester MBA	IV semester B.E./B.Tech	II semester B.Sc.	I sem B.E./B.Tech./ B.Plan/B.Arch (Revised)
Commencement of Semester	04.04.2022	04.04.2022	09.05.2022	16.05.2022	23.05.2022	13.12.2021
Last Working day of Semester	16.07.2022	16.07.2022	20.08.2022	27.08.2022	05.09.2022	10.05.2022
Practical/Viva-Examination	18.07.2022 To 29.07.2022	18.07.2022 To 29.07.2022	----	01.09.2022 To 08.09.2022	06.09.2022 To 09.09.2022	28.05.2022 To 04.06.2022
Theory Examinations	01.08.2022 To 20.08.2022	01.08.2022 To 20.08.2022	22.08.2022 To 14.09.2022	12.09.2022 To 30.09.2022	12.09.2022 To 28.09.2022	12.05.2022 To 27.05.2022
Internship	21.08.2022 To 10.09.2022	21.08.2022 To 10.09.2022	---	---	---	
Internship Viva-Voce/ Project viva	---	---	---	---	---	
Summer Project / Professional training / Organization Study	---	---	---	---	---	
Submission of the report to University	----	---	11.07.2022 To 22.07.2022	---	---	
Commencement of NEXT Semester	19.09.2022	19.09.2022	----	10.10.2022	10.10.2022	06.06.2022

Please Note:

- The academic sessions for EVEN semesters should commence from the dates mentioned above.
- All the students of VI semesters B.E./B.Tech. programs have to join the VII semester after completion of their **INTERNSHIP** during the above-mentioned duration.
- **The Institute/Department shall plan to have extra classes to complete the requisite hours of teaching and learning as per the scheme.**
- Faculty should conduct additional tutorial classes in blended mode to solve the doubts of the students.

Professor & Head
Dept. of Electronics & Communication Engg
Adichunchanagiri Institute of Technology,
Chikmagalur - 57...

...ulty should conduct additional tutorial classes in blended mode to solve the doubts of the students.

- The faculty/staff shall be available to undertake any work assigned by the university.
- Notification regarding the Calendar of Events relating to the conduction of University Examinations will be issued by the Registrar (Evaluation) from time to time.
- Academic Calendar **may be modified** based on guidelines/directions issued in the future by MHRD/UGC/AICTE/State Government.
- Academic Calendar is also applicable for **Autonomous Colleges.** In case any changes are to be effected by Autonomous Colleges in the academic terms and examination schedule, they could do so with the approval of the University.

REGISTRAR

Professor & Head
Dept. of Electronics & Communication Engg
Adichunchanagiri Institute of Technology
Chikmagalur - 577 102

...3/3

Academic Calendar for ODD Semester of UG programmes for year 2021-22

	V semester B.E./B.Tech.	V semester B.Arch./ B.Plan.	VII semester B.E./B.Tech.	VII semester B.Plan./B.Arch	IX semester B.Arch	III semester B.E./ B.Tech.	III Semester B.Arch.	III semester B. Plan	I semester B.E./B.Tech.	I semester B.Arch/B.Plan
Commencement of ODD Semester	01.10.2021	01.10.2021	01.10.2021	01.10.2021	01.10.2021	18.10.2021	18.10.2021	18.10.2021	Will be announced later	
Last Working day of ODD Semester	31.01.2022	31.01.2022	31.01.2022	31.01.2022	31.01.2022	19.02.2022	19.02.2022	19.02.2022		
Practical Examination	01.02.2022 To 10.02.2022	01.02.2022 To 10.02.2022	01.02.2022 To 10.02.2022	01.02.2022 To 10.02.2022	---	21.02.2022 To 04.03.2022	21.02.2022 To 04.03.2022	21.02.2022 To 04.03.2022		
Theory Examinations	11.02.2022 To 25.03.2022	11.02.2022 To 25.03.2022	11.02.2022 To 25.03.2022	11.02.2022 To 25.03.2022	---	07.03.2022 To 25.03.2022	07.03.2022 To 25.03.2022	07.03.2022 To 25.03.2022		
Internship	---	---	---	---	---	---	---	---		
Internship Viva Voce/ Project viva	---	---	---	---	---	---	---	---		
Summer Project / Professional training / Organization Study	---	---	---	---	---	---	---	---		
Submission of the report to University	---	---	---	---	---	---	---	---		
Commencement of EVEN Semester	04.04.2022	04.04.2022	04.04.2022	04.04.2022	07.02.2022	11.04.2022	11.04.2022	11.04.2022		

Professor & Head
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Chikmagalur - 577 102

Academic Calendar for IV sem MBA / IV semB.E./B.Tech.(Revised) VI sem B.E./B.Tech /B.Plan., (Revised) B.E./B.Tech./B.Arch./B.Plan., and II sem B.Sc. Programs for AY-2021-22

	VI semester B.E./B.Tech. (Revised)	VI semester B.Plan. (Revised)	IV Semester MBA	IV semester B.E./B.Tech	II semester B.Sc.	I sem B.E./B.Tech./ B.Plan/B.Arch (Revised)
Commencement of Semester	04.04.2022	04.04.2022	09.05.2022	16.05.2022	23.05.2022	13.12.2021
Last Working day of Semester	16.07.2022	16.07.2022	20.08.2022	27.08.2022	05.09.2022	10.05.2022
Practical/Viva-Examination	18.07.2022 To 29.07.2022	18.07.2022 To 29.07.2022	----	01.09.2022 To 08.09.2022	06.09.2022 To 09.09.2022	28.05.2022 To 04.06.2022
Theory Examinations	01.08.2022 To 20.08.2022	01.08.2022 To 20.08.2022	22.08.2022 To 14.09.2022	12.09.2022 To 30.09.2022	12.09.2022 To 28.09.2022	12.05.2022 To 27.05.2022
Internship	21.08.2022 To 10.09.2022	21.08.2022 To 10.09.2022	---	---	---	
Internship Viva-Voce/ Project viva	---	---	---	---	---	
Summer Project / Professional training / Organization Study	---	---	----	---	----	
Submission of the report to University	----	---	11.07.2022 To 22.07.2022	---	---	
Commencement of NEXT Semester	19.09.2022	19.09.2022	----	10.10.2022	10.10.2022	06.06.2022

Please Note:

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Adichunchanagiri Institute of Technology,
Chikmagalur - 577 102

||JAI SRI GURUDEV||

AIT	College Calendar of Events	Format No.	ACD01
		Issue No.	01
		Rev. No.	00

Academic Year : 2021-2022 **Semester :Even**

Sl No.	Date	Event	Remarks
1	4 Apr 2022	Commencement of 6th and 8th semester B.E. classes.	
2	14 Apr 2022	Holiday, Mahaveer Jayanthi, Ambedkar Jayanthi	
3	3 May 2022	Holiday, Basava Jayanthi, Ramzan	
4	21 May 2022	First Test Cycle for 8th semester B.E. Students	
5	23 May 2022	Commencement of 3rd semester B.E. classes.	
6	27 May 2022 to 29 May 2022	First Test Cycle for 6th semester B.E. Students	
7	30 May 2022	Workshop on "Importance of Administrative tasks " for non-teaching staff	
8	6 June 2022	Commencement of 2nd semester B.E. classes.	
9	10 June 2022	Second Test Cycle for 8th semester B.E. Students	
10	14 June 2022	Ethnic Day for 8th semester Students	
11	15 June 2022	Induction Program for first year Students	
12	16 June 2022	Graduation Day for 8th semester Students	
13	17 June 2022 & 18 June 2022	Chunchana-2022	
14	25 June 2022 to 27 June 2022	Second Test Cycle for 6th semester B.E. Students	
15	30 June 2022	Third Test Cycle for 8th semester B.E. Students. Last Working Day for 8th semester B.E. classes.	
16	1 July 2022 to 3 July 2022	First Test Cycle for 4th and 2nd semester B.E. Students	
17	4 July 2022 to 20 July 2022	Theory Examinations for 8th semester B.E. Students	

18	14 July 2022 to 16 July 2022	Third Test Cycle for 6th semester B.E. Students	
19	16 July 2022	Last Working Day for 6th semester B.E. classes.	
20	18 July 2022 to 29 July 2022	Practical Examinations for 6th semester B.E. Students	
21	21 July 2022 to 30 July 2022	Internship viva-voce/Project Viva for 8th Semester Students	
22	31 July 2022 to 2 Aug 2022	Second Test Cycle for 4th and 2nd semester B.E. Students	
23	1 Aug 2022 to 20 Aug 2022	Theory Examinations for 6th semester B.E. Students	
24	9 Aug 2022	Holiday, Muharram	
25	15 Aug 2022	Holiday, Independence Day	
26	27 Aug 2022 to 29 Aug 2022	Third Test Cycle for 4th and 2nd semester B.E. Students	
27	31 Aug 2022	Holiday, Ganesha Chaturthi	
28	1 Sept 2022 to 8 Sept 2022	Practical Examinations for 4th semester B.E. Students	
29	11 Sept 2022 to 29 Sept 2022	Theory Examinations for 2nd semester B.E. Students	
30	12 Sept 2022 to 30 Sept 2022	Theory Examinations for 4th semester B.E. Students	
31	1 Oct 2022 to 10 Oct 2022	Practical Examinations for 2nd semester B.E. Students	

Note: Add any other events like Guest Lecture, National/International Conference ,Seminars, etc in individual department calendar of events .

Copy to:

1. **All HOD's**
2. **Placement Officer**
3. **Establishment Section**
4. **Dhi Team**

PRINCIPAL
AIT, Chickmagalur

Professor & Head
Dept. of Electronics & Communication Engg.
Adichunchanagiri Institute of Technology
Chikmagalur - 577 102

|| Jai Sri Gurudev ||

Sri Adichunchanagiri Shikshana Trust ®

Adichunchanagiri Institute of Technology, Chikkamagaluru

AIT/A2/ 573/2022-23 Date: 02.06.2022

CIRCULAR

As per the VTU Notification, the 2nd sem. B.E Classes will re-open on 06.06.2022. The students are here by informed to attend the classes regularly without fail.

Dr. C.T. JAYADEVA
Principal B.E.,M.Tech.,Ph.D.
Adichunchanagiri Institute of Technology
CHIKKAMAGALURU-577102

Copy to:

1. All HOD's
2. All Department NB
3. Boys Hostel
4. Girls Hostel
5. HRD
6. Admission section

Professor & Head
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Chikmagalur - 577 102

||Jai Sri Gurudev||

Adichunchanagiri Shikshana Trust (R)

Adichunchanagiri Institute of Technology, Chikmagalur - 577102

Date: 04-05-2022

Internal Test Schedule for eighth Semester

1st Test Cycle

DATE	21-05-2022	21-05-2022
DAY	Saturday	Saturday
TIME	09.00 AM to 10.00 AM	12.00 PM to 01.00 PM
Subject Code	18XX81	18XX82X

2nd Test Cycle

DATE	10-06-2022	10-06-2022
DAY	Friday	Friday
TIME	09.00 AM to 10.00 AM	12.00 PM to 01.00 PM
Subject Code	18XX81	18XX82X

3rd Test Cycle

DATE	30-06-2022	30-06-2022
DAY	Thursday	Thursday
TIME	09.00 AM to 10.00 AM	12.00 PM to 01.00 PM
Subject Code	18XX81	18XX82X

Professor & Head
Dept. of Electronics & Communication Engg
Adichunchanagiri Institute of Technology
Chikmagalur - 577 102

TCM Co-ordinators: R&M

Dr. C. T. JAYADEVA
Principal
B.E., M.Tech., Ph.D.
Adichunchanagiri Institute of Technology
CHIKKAMAGALURU-577102

Adichunchanagiri Shikshana Trust (R)

Adichunchanagiri Institute of Technology, Chikmagalur - 577102

Date: 04-05-2022

Internal Test Schedule for Sixth Semester

1st Test Cycle

DATE	27-05-2022	27-05-2022	28-05-2022	28-05-2022	29-05-2022
DAY	Friday	Friday	Saturday	Saturday	Sunday
TIME	09.00 AM to 10.00 AM	12.00 PM to 01.00 PM	09.00 AM to 10.00 AM	12.00 PM to 01.00 PM	09.00 AM to 10.00 AM
Subject Code	18XX61	18XX62	18XX63	18XX64X	18XX65X

2nd Test Cycle

DATE	25-06-2022	25-06-2022	26-06-2022	26-06-2022	27-06-2022
DAY	Saturday	Saturday	Sunday	Sunday	Monday
TIME	09.00 AM to 10.00 AM	12.00 PM to 01.00 PM	09.00 AM to 10.00 AM	12.00 PM to 01.00 PM	09.00 AM to 10.00 AM
Subject Code	18XX61	18XX62	18XX63	18XX64X	18XX65X

3rd Test Cycle

DATE	14-07-2022	14-07-2022	15-07-2022	15-07-2022	16-07-2022
DAY	Thursday	Thursday	Friday	Friday	Saturday
TIME	09.00 AM to 10.00 AM	12.00 PM to 01.00 PM	09.00 AM to 10.00 AM	12.00 PM to 01.00 PM	09.00 AM to 10.00 AM
Subject Code	18XX61	18XX62	18XX63	18XX64X	18XX65X

Test Co-ordinator : Mr RSM

Professor & Head
Dept. of Electronics & Communication Engg
Adichunchanagiri Institute of Technology
Chikmagalur - 577 102

Dr. C. T. JAYADEVA
Principal
Principal Tech. Ph.D.
Adichunchanagiri Institute of Technol
CHIKKAMAGALURU-577102

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Internal Test Schedule for Fourth Semester

Date: 02-06-2022

1st Test Cycle

DATE	01-07-2022	01-07-2022	01-07-2022	02-07-2022	02-07-2022	03-07-2022	03-07-2022
DAY	Friday	Friday	Friday	Saturday	Saturday	Sunday	Sunday
TIME	09.00 AM to 10.00 AM	12.00 PM to 01.00 PM	03.30 PM to 04.30 PM	09.00 AM to 10.00 AM	12.00 PM to 01.00 PM	09.00 AM to 10.00 AM	12.00 PM to 01.00 PM
Subject Code	18MAT41	18XX42	18KVK/KAK/CPC 49	18XX43	18XX44	18XX45	18XX46

2nd Test Cycle

DATE	31-07-2022	31-07-2022	01-08-2022	01-08-2022	02-08-2022	02-08-2022	02-08-2022
DAY	Sunday	Sunday	Monday	Monday	Tuesday	Tuesday	Tuesday
TIME	09.00 AM to 10.00 AM	12.00 PM to 01.00 PM	09.00 AM to 10.00 AM	12.00 PM to 01.00 PM	09.00 AM to 10.00 AM	12.00 PM to 01.00 PM	03.30 PM to 04.30 PM
Subject Code	18MAT41	18XX42	18XX43	18XX44	18XX45	18XX46	18KVK/KAK/CPC 49

3rd Test Cycle

DATE	27-08-2022	27-08-2022	28-08-2022	28-08-2022	29-08-2022	29-08-2022	29-08-2022
DAY	Saturday	Saturday	Sunday	Sunday	Monday	Monday	Monday
TIME	09.00 AM to 10.00 AM	12.00 PM to 01.00 PM	09.00 AM to 10.00 AM	12.00 PM to 01.00 PM	09.00 AM to 10.00 AM	12.00 PM to 01.00 PM	03.30 PM to 04.30 PM
Subject Code	18MAT41	18XX42	18XX43	18XX44	18XX45	18XX46	18KVK/KAK/CPC 49

Professor & Head
Dept. of Electronics & Communication Engg
Adichunchanagiri Institute of Technology,
Chikmagalur - 577 102

Dr. C.T. JAYADEVA
Principal
B.E.,M.Tech.,Ph.D.
Principal
Adichunchanagiri Institute of Technology
CHIKKAMAGALURU-577102

||Jai Sri Gurudev ||

Adichunchanagiri Shikshana Trust (R)

Adichunchanagiri Institute of Technology, Chikmagalur - 577102

Internal Test Schedule for Second Semester Physics Cycle

Date: 09-06-2022

1st Test Cycle

DATE	01-07-2022	01-07-2022	02-07-2022	02-07-2022
DAY	Friday	Friday	Saturday	Saturday
TIME	09.00 AM to 10.00 AM	12.00 PM to 01.00 PM	09.00 AM to 10.00 AM	12.00 PM to 01.00 PM
Subject Code	21MAT21	21PHY22	21ELE23	21CIV24

2nd Test Cycle

DATE	31-07-2022	31-07-2022	01-08-2022	01-08-2022
DAY	Sunday	Sunday	Monday	Monday
TIME	09.00 AM to 10.00 AM	12.00 PM to 01.00 PM	09.00 AM to 10.00 AM	12.00 PM to 01.00 PM
Subject Code	21MAT21	21PHY22	21ELE23	21CIV24

3rd Test Cycle

DATE	27-08-2022	27-08-2022	28-08-2022	28-08-2022
DAY	Saturday	Saturday	Sunday	Sunday
TIME	09.00 AM to 10.00 AM	12.00 PM to 01.00 PM	09.00 AM to 10.00 AM	12.00 PM to 01.00 PM
Subject Code	21MAT21	21PHY22	21ELE23	21CIV24

Professor & Head
Dept. of Electronics & Communication Engg
Adichunchanagiri Institute of Technology,
Chikmagalur - 577 102

Dr. C. T. JAYADEVA
Principal
B.E., M.Tech., Ph.D.
Adichunchanagiri Institute of Technology
CHIKKAMAGALURU-577102

||Jai Sri Gurudev ||

Adichunchanagiri Shikshana Trust (R)

Adichunchanagiri Institute of Technology, Chikmagalur - 577102

Internal Test Schedule for Second Semester Chemistry Cycle

Date: 09-06-2022

1st Test Cycle

DATE	01-07-2022	01-07-2022	02-07-2022	02-07-2022	03-07-2022
DAY	Friday	Friday	Saturday	Saturday	Sunday
TIME	09.00 AM to 10.00 AM	12.00 PM to 01.00 PM	09.00 AM to 10.00 AM	12.00 PM to 01.00 PM	09.00 AM to 10.00 AM
Subject Code	21MAT21	21PSP23	21CHE22	21ELN24	21EME25

2nd Test Cycle

DATE	31-07-2022	31-07-2022	01-08-2022	01-08-2022	02-08-2022
DAY	Sunday	Sunday	Monday	Monday	Tuesday
TIME	09.00 AM to 10.00 AM	12.00 PM to 01.00 PM	09.00 AM to 10.00 AM	12.00 PM to 01.00 PM	09.00 AM to 10.00 AM
Subject Code	21MAT21	21PSP23	21CHE22	21ELN24	21EME25

3rd Test Cycle

DATE	27-08-2022	27-08-2022	28-08-2022	28-08-2022	29-08-2022
DAY	Saturday	Saturday	Sunday	Sunday	Monday
TIME	09.00 AM to 10.00 AM	12.00 PM to 01.00 PM	09.00 AM to 10.00 AM	12.00 PM to 01.00 PM	09.00 AM to 10.00 AM
Subject Code	21MAT21	21PSP23	21CHE22	21ELN24	21EME25

Professor & Head
Dept. of Electronics & Communication Engg
Adichunchanagiri Institute of Technology,
Chikmagalur - 577 102

Dr. C. T. JAYADEVA
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ADICHUNCHANAGIRI INSTITUTE OF TECHNOLOGY

Electronics & Communication Engineering (EC)

Course Name : MICROCONTROLLER LABORATORY (18ECL47)

Class : Semester 4 B (Batch 3)

Ms Divya G S,
Assistant Professor,

2021-22

Professor & Head
Dept. of Electronics & Communication Engg
Adichunchanagiri Institute of Technology
Chikmagalur - 577 102

2 . Course Allotted

Allotted Duty	Course Title	Course Code
Lab 1	MICROCONTROLLER LABORATORY	18ECL47

HOD

ADICHUNCHANAGIRI INSTITUTE OF TECHNOLOGY

Department of Electronics & Communication Engineering (EC)

Date	Day	Event
8 Aug 2022	MONDAY	exam
9 Aug 2022	TUESDAY	Moharam
9 Aug 2022	TUESDAY	exam
10 Aug 2022	WEDNESDAY	exam
11 Aug 2022	THURSDAY	exam
12 Aug 2022	FRIDAY	exam
13 Aug 2022	SATURDAY	exam
14 Aug 2022	SUNDAY	exam
15 Aug 2022	MONDAY	Independence Day
15 Aug 2022	MONDAY	exam
16 Aug 2022	TUESDAY	exam
17 Aug 2022	WEDNESDAY	exam
18 Aug 2022	THURSDAY	exam
19 Aug 2022	FRIDAY	exam
20 Aug 2022	SATURDAY	exam
21 Aug 2022	SUNDAY	exam
22 Aug 2022	MONDAY	exam
31 Aug 2022	WEDNESDAY	Ganesh Chathruthi
3 Sep 2022	SATURDAY	Term End Date

5 . Department Details

5 . 1 Preliminary Information

PROGRAM OUTCOMES(PO's)

1. **Engineering knowledge :** Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.

2. **Problem analysis :** Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.

3. **Design/development of solutions :** Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.

4. **Conduct investigations of complex problems :** Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.

5. **Modern tool usage :** Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.

6. **The engineer and society :** Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.

7. **Environment and sustainability :** Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.

8. **Ethics :** Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.

9. **Individual and team work :** Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.

10. **Communication :** Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.

11. **Project management and finance :** Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.

12. **Life-long learning :** Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change

6 . Course Information

6 . 1 Course Content

Title of the Course : MICROCONTROLLER LABORATORY
Semester : 4 **Academic Year : 2021-22**

Subject Code : 18ECL47	IA Marks : 40
Hours/week : 4	Total Hours : 40
Exam Hours : 3	Exam Marks : 60
Course Plan Author : -	Planned Date : -
Approved by : -	Approved Date : -

Objectives:

1 . Understand the basics of microcontroller and its applications.

2 . Have in-depth knowledge of 8051 assembly language programming.

3 . Understand controlling the devices using C programming.

4 . The concepts of I/O interfacing for developing real time embedded systems.

Course Outcomes (COs) :

1 . Identify and state the instructions of 8051 for performing data transfer, arithmetic, Boolean, logical and interrupt operations.

2 . Write down assembly language programs using the instruction set of 8051 for manipulating the input data.

3 . Demonstrate the interfacing of different peripheral devices to 8051 through I/O ports and control those using Assembly language programs.

4 . Demonstrate the interfacing of 8051 to perform the serial data transfer using C programming.

5 . Demonstrate the functionalities of on-chip peripherals such as timer/counter of microcontroller through assembly language programming.

Experiment - 12

Write ALP to interface a Stepper Motor to 8051 to rotate the motor.

Experiment - 13

Write ALP to interface ADC-0804 and convert an analog input connected to it.

ADICHUNCHANAGIRI INSTITUTE OF TECHNOLOGY

Department of Electronics & Communication Engineering (EC)

Daily Lab Score

USN	Name	Exp 1	Exp 2	Exp 3	Exp 4	Exp 5	Exp 6	Exp 7	Exp 8	Exp 9	Exp 10	Exp 11	Exp 12	Exp 13	Aggregate
4AI20EC096	Sujay Urs C B	1	1	0	0	0	0	0	0	0	0	0	0	0	1
4AI20EC097	Sukhi D	23	23	23	23	23	23	23	23	23	23	23	23	23	23
4AI20EC098	Swamy Kotresh B	20	18	20	20	20	20	20	20	20	20	20	20	20	20
4AI20EC099	Swarna Gowri K S	23	23	23	23	23	21	23	23	23	23	23	23	23	23
4AI20EC100	Swathi B P	23	23	23	23	23	23	23	23	23	23	23	23	23	23
4AI20EC101	Swathisha H Shetty	22	22	22	22	21	22	22	22	22	22	22	22	22	22
4AI20EC102	Vagdevi M K	20	20	20	20	20	20	20	20	20	20	20	20	20	20
4AI20EC103	Vaishnavi S R	22	21	22	21	23	23	23	23	22	21	21	22	21	22
4AI20EC104	Varsha C J	23	23	23	23	23	23	23	23	23	23	23	23	23	23
4AI20EC105	Varshini S	23	23	23	23	23	23	23	23	23	23	23	23	23	23
4AI20EC106	Varshith D N	23	23	23	23	23	23	23	23	23	23	22	23	23	23
4AI20EC107	Varshitha S V	23	23	23	23	23	23	23	23	23	23	23	22	22	23
4AI20EC108	Vedhashree C R	23	23	23	23	23	23	23	21	23	23	23	23	23	23
4AI20EC109	Vinayak Bhyresh Onimani	0	1	1	1	3	1	0	0	0	0	0	0	0	1
4AI20EC110	Vinayaka M S	18	18	18	18	18	18	18	18	18	18	18	18	18	18
4AI20EC111	Vivek S M	24	24	24	24	24	24	24	24	24	24	24	24	24	24
4AI20EC112	Yashwanth K N	23	23	23	23	23	23	23	23	22	22	22	23	23	23
4AI20EC113	Yogish N S	15	16	16	16	16	16	16	16	16	16	16	16	16	16

6 . Course Information

6 . 2 . 3 CO-PSO Mapping

Slight (Low) = 1 , Moderate (Medium) = 2 , Substantial (High) = 3 .

CO/PSO	PSO 1	PSO 2
CO 1	2	2
CO 2	2	2
CO 3	2	2
CO 4	2	2
CO 5	2	2

HOD

6 . Course Information

6 . 2 . 2 CO PO Mapping

Slight (Low) = 1 , Moderate (Medium) = 2 , Substantial (High) = 3 .

CO/ PO	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12
CO 1	3	2	3									
CO 2	3	2	3		2							
CO 3	2	2	2		2							
CO 4	2	2	2		2							
CO 5	2	2	2		2							

HOD

6 . Course Information

6 . 4 Internal Assessment

Internal : 1

Semester:4-CBCS 2018 | Date : 26/08/2022

Subject : MICROCONTROLLER LABORATORY (18ECL47) | Time : 14:00 - 17:00

Faculty : Divya | Max Marks: 16

Sl#	Experiment #	Experiment	CO
1	1	Data Transfer: Block Move, Exchange, Sorting, Finding largest element in an array.	1 , 2
2	2	Arithmetic Instructions - Addition\/subtraction, multiplication and division, square, Cube \u2013 (16 bits Arithmetic operations \u2013 bit addressable).	1 , 2
3	3	Counters	1 , 2
4	4	Boolean & Logical Instructions (Bit manipulations).	1 , 2
5	6	Code conversion: BCD \u2013 ASCII; ASCII \u2013 Decimal; Decimal - ASCII; HEX - Decimal and Decimal - HEX	1 , 2
6	5	Conditional CALL & RETURN.	2 , 1
7	7	Programs to generate delay, Programs using serial port and on-Chip timer\/counter.	5
8	8	Interface a simple toggle switch to 8051 and write an ALP to generate an interrupt which switches on an LED (i) continuously as long as switch is on and (ii) only once for a small time when the switch isturned on.	1 , 3
9	9	Write a C program to (i) transmit and (ii) to receive a set of characters serially by interfacing 8051 to a terminal.	4
10	10	Write ALPs to generate waveforms using DAC interface.	3
11	12	Write ALP to interface a Stepper Motor to 8051 to rotate the motor.	3

Evaluation

USN	Name	Present (P) / Absent (Ab)	Experiment	IA Total
4AI20EC096	Sujay Urs C B	P	1 , 12	4
4AI20EC097	Sukhi D	P	1 , 3	12

ADICHUNCHANAGIRI INSTITUTE OF TECHNOLOGY

Department of Electronics & Communication Engineering (EC)

USN	Name	Present (P) / Absent (Ab)	Experiment	IA Total
4AI20EC098	Swamy Kotresh B	P	6 , 9	4
4AI20EC099	Swarna Gowri K S	P	7 , 8	16
4AI20EC100	Swathi B P	P	6 , 12	16
4AI20EC101	Swathisha H Shetty	P	4 , 10	10
4AI20EC102	Vagdevi M K	P	6 , 9	6
4AI20EC103	Vaishnavi S R	P	7 , 9	16
4AI20EC104	Varsha C J	P	1 , 12	16
4AI20EC105	Varshini S	P	3 , 8	12
4AI20EC106	Varshith D N	P	4 , 10	16
4AI20EC107	Varshitha S V	P	6 , 12	15
4AI20EC108	Vedhashree C R	P	5 , 8	13
4AI20EC109	Vinayak Bhyresh Onimani	P	2 , 7	4
4AI20EC110	Vinayaka M S	P	5 , 7	4
4AI20EC111	Vivek S M	P	8 , 12	16
4AI20EC112	Yashwanth K N	P	5 , 7	8
4AI20EC113	Yogish N S	P	10 , 1	6

Adichunchanagiri Institute of Technology,
Chikkamagaluru-2

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

COURSE OBJECTIVES AND OUTCOMES-2021-22

Course Title : MICROCONTROLLER LABORATORY **Course Code : 18ECL47**

No. of Lecture Hrs./Week : 02Hr Tutorial (Instructions)
+ 02 Hours Laboratory

Exam Hours : 03

Exam Marks : 80

Prerequisites

1. Computer Organization
2. Digital Electronics

Course Learning Objectives

This laboratory course enables students to

- Understand the basics of microcontroller and its applications.
- Have in-depth knowledge of 8051 assembly language programming.
- Understand serial communication through the devices using C programming.
- Understand the concepts of I/O interfacing for 8051.

Course Outcomes:

On the completion of this laboratory course, the students will be able to:

CO Number	Course Outcomes	RBT Level
18ECL47.1	Identify and state the instructions of 8051 for performing data transfer, arithmetic, Boolean, logical and interrupt operations.	L1
18ECL47.2	Write down assembly language programs using the instruction set of 8051 for manipulating the input data.	L1,L2
18ECL47.3	Demonstrate the interfacing of different peripheral devices to 8051 through I/O ports and control those using Assembly language programs.	L3
18ECL47.4	Demonstrate the interfacing of 8051 to perform the serial data transfer using C programming.	L3
18ECL47.5	Demonstrate the functionalities of on-chip peripherals such as timer/counter of microcontroller through assembly language programming.	L3

CO-PO MAPPING 2019-2020

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12		PSO1	PSO2
18ECL47.1	3	2	3											2	2
18ECL47.2	3	2	3		2									2	2
18ECL47.3	2	2	2		2									2	2
18ECL47.4	2	2	2		2									2	2
18ECL47.5	2	2	2		2									2	2

CO-PO MAPPING JUSTIFICATION

18ECL47	18ECL47.1	PO1	3	Apply the knowledge of fundamentals of digital electronics to provide the solution for the design of embedded system.
		PO2	2	Apply the knowledge to analyze the problem .
		PO3	3	Apply the knowledge for the design of embedded system.
	18ECL47.2	PO1	3	Apply the knowledge of instruction set to develop the assembly language program
		PO2	2	Apply the knowledge to write down the assembly language programs for solving problems.
		PO3	3	Apply the knowledge of ALP to develop solutions for problems.
		PO5	2	Assemblers and Compilers are used to write and execute ALPs.
	18ECL47.3	PO1	2	Apply the knowledge of peripheral devices so as to interface with the microcontroller.
		PO2	2	Apply the knowledge of microcontroller for analyzing the interfaced peripherals.
		PO3	2	Apply the knowledge of interfacing for the design of embedded system.
		PO5	2	Assemblers and Compilers are used to demonstrate the interfacing of the peripheral devices with microcontrollers and control them.
	18ECL47.4	PO1	2	Apply the knowledge of serial communication for data transfer through serial port of 8051.
		PO2	2	Apply the knowledge of C programming to solve the problems in serial communication.
		PO3	2	Apply the knowledge of serial communication for the design of embedded system.
		PO5	2	Assemblers and Compilers are used to perform the serial communication with microcontrollers.
	18ECL47.5	PO1	2	Apply the knowledge of assembly language and C programming to

				understand the features of microcontroller.
		PO2	2	Apply the knowledge to solve the problems of microcontroller based applications.
		PO3	2	Apply the knowledge of assembly language and C programming for the design of embedded system.
		PO5	2	Assemblers and Compilers are used to demonstrate the functionalities of microcontrollers.

CO-PSO MAPPING JUSTIFICATION

18ECL47	18ECL47.1	PSO1	2	Graduates are able to analyse the instruction set of microcontroller to develop the code for meeting the requirement specification of a embedded system.
		PSO2	2	Graduates are able to write an efficient program by minimizing the length of the ALP.
	18ECL47.2	PSO1	2	Graduates are able to develop the assembly language programs for embedded system according to required specifications .
		PSO2	2	Graduates are able to provide a solution by developing an efficient program for an embedded system
	18ECL47.3	PSO1	2	Graduates are able to demonstrate the interfacing of peripheral devices with microcontroller to build an embedded system
		PSO2	2	Graduates are able to identify the issues and resolve them while interfacing the peripheral devices with microcontroller.
	18ECL47.4	PSO1	2	Graduates are able to demonstrate the serial communication for data transfer between the devices in the development of an embedded system.
		PSO2	2	Graduates are able to identify the issues with the serial communication between the peripheral devices and microcomputer and resolve them.
	18ECL47.5	PSO1	2	Graduates are able to analyse the functionalities of timers/counters in an embedded system.
		PSO2	2	Graduates are able to provide a solution by programming the on-chip timers/counters according to the requirements for an embedded system.

Signature of the Lab co-ordinator

Signature of the Module Co-ordinator

Signature of the HOD

Rubrics for lab-Evaluation

Parameters	*Good (7-8)*	*Satisfactory(4-6)*	*Poor(0-3)*
Pre-lab preparation (8)	Good Knowledge about the controller, experiment to be conducted & prior write up.	Not much Knowledge & no proper prior write up.	No knowledge & no prior write up.
Conduction & results (8)	Analyzed the program and able to interpret the results well.	Analyzed the program partially and results not presented correctly.	Unable to analyze the program and results not presented.
Record write up & regular submission (8)	Program write up is presented well with appropriate comments. Regular in record submission.	Program write up is presented without appropriate comments. Not regular in record submission.	No record write up or record not submitted
Test(16)			
Total = 40 marks			

Laboratory Experiments

I. PROGRAMMING

1. Data Transfer: Block Move, Exchange, Sorting, Finding largest element in an array.
2. Arithmetic Instructions - Addition/subtraction, multiplication and division, square, Cube – (16 bits Arithmetic operations – bit addressable).
3. Counters.
4. Boolean & Logical Instructions (Bit manipulations).
5. Conditional CALL & RETURN.
6. Code conversion: BCD – ASCII; ASCII – Decimal; Decimal - ASCII; HEX - Decimal and Decimal - HEX.
7. Programs to generate delay using serial port and on-Chip timer/counter.

II. INTERFACING

1. Interface a simple toggle switch to 8051 and write an ALP to generate an interrupt which switches on an LED (i) continuously as long as switch is on and (ii) only once for a small time when the switch is turned on.
2. Write a C program to (i) transmit and (ii) to receive a set of characters serially by interfacing 8051 to a terminal.
3. Write ALPs to generate waveforms using DAC interface.
4. Write ALP to interface an LCD display and to display a message on it.
5. Write ALP to interface a Stepper Motor to 8051 to rotate the motor.
6. Write ALP to interface ADC-0804 and convert an analog input connected to it.

ADICHUNCHANAGIRI INSTITUTE OF TECHNOLOGY

Electronics & Communication Engineering (EC)

Course Name : MICROCONTROLLER (18EC46)

Class : Semester 4 B

Professor & Head
Dept. of Electronics & Communication Engg
Adichunchanagiri Institute of Technology
Chikmagalur - 577 102

Ms Divya G S,
Assistant Professor,
2021-22

2 . Course Allotted

Allotted Duty	Course Title	Course Code
Theory 1	MICROCONTROLLER	18EC46

HOD

ADICHUNCHANAGIRI INSTITUTE OF TECHNOLOGY

Department of Electronics & Communication Engineering (EC)

Date	Day	Event
8 Aug 2022	MONDAY	exam
9 Aug 2022	TUESDAY	Moharam
9 Aug 2022	TUESDAY	exam
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15 Aug 2022	MONDAY	exam
16 Aug 2022	TUESDAY	exam
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18 Aug 2022	THURSDAY	exam
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20 Aug 2022	SATURDAY	exam
21 Aug 2022	SUNDAY	exam
22 Aug 2022	MONDAY	exam
31 Aug 2022	WEDNESDAY	Ganesh Chathruthi
3 Sep 2022	SATURDAY	Term End Date

4 . Timetable

	1	2	3	4		5	6	7
	09:00 AM 10:00 AM	10:00 AM 11:00 AM	11:15 AM 12:15 PM	12:15 PM 01:15 PM	01:15 PM 02:30 PM	02:30 PM 03:20 PM	03:20 PM 04:10 PM	04:10 PM 05:00 PM
MON		BE 18EC46 EC Semester 4 B				BE 18ECL47 EC Semester 4 B		
TUE	BE 18EC652 CS Semester 6 A		BE 18EC46 EC Semester 4 B					
WED			BE 18EC652 CS Semester 6 A					
THU	BE 18ECL47 EC Semester 4 B			BE 18EC652 CS Semester 6 A				BE 18EC46 EC Semester 4 B
FRI		BE 18EC46 EC Semester 4 B				BE 18ECL47 EC Semester 4 B		
SAT								

HOD

5 . Department Details

5 . 1 Preliminary Information

PROGRAM OUTCOMES(PO's)

1. **Engineering knowledge :** Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.

2. **Problem analysis :** Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.

3. **Design/development of solutions :** Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.

4. **Conduct investigations of complex problems :** Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.

5. **Modern tool usage :** Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.

6. **The engineer and society :** Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.

7. **Environment and sustainability :** Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.

8. **Ethics :** Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.

9. **Individual and team work :** Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.

10. **Communication :** Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.

11. **Project management and finance :** Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.

12. **Life-long learning :** Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change

ADICHUNCHANAGIRI INSTITUTE OF TECHNOLOGY

Department of Electronics & Communication Engineering (EC)

6 . Course Information

6 . 1 Course Content

Title of the Course : MICROCONTROLLER
Semester : 4

Academic Year : 2021-22

Subject Code : 18EC46	IA Marks : 40
Hours/week : 3	Total Hours : 50
Exam Hours : 3	Exam Marks : 60
Course Plan Author : Divya	Planned Date : 2022-10-10
Approved by : Dr Goutham M A	Approved Date : 2022-10-10

Objectives:

1 . Understand the difference between a Microprocessor and a Microcontroller and embedded microcontrollers.

2 . Familiarize the basic architecture of 8051 microcontroller.

3 . Program 8051microprocessor using Assembly Level Language and C.

4 . Understand the interrupt system of 8051 and the use of interrupts.

5 . Understand the operation and use of inbuilt Timers/Counters and Serial port of 8051.

6 . Interface 8051 to external memory and I/O devices using its I/O ports.

Course Outcomes (COs) :

1 . Able to list the difference between Microprocessor and Microcontrollers and explain the architecture of 8051 microcontroller

2 . Able to identify the various instructions, explain the operation performed by the instructions, stack and subroutines and write assembly language programmes, I\O port interfacing programmes

3 . Able to explain the working of 8051 on-chip peripherals like interrupt system, timers\counters and serial ports\parallel ports and write 8051 assembly language programs and C programs for their working

4 . Able to illustrate interfacing of external memory, simple switches, simple LED's, ADC 0804, LCD and stepper motor to 8051, and write assembly programmes

6 . Course Information

6 . 1 . 1 Course Syllabus

Objectives:
Title of the Course : MICROCONTROLLER
Subject Code : 18EC46

Module 1

8051 Microcontroller :

Microprocessor Vs Microcontroller, Embedded Systems, Embedded Microcontrollers, 8051 Architecture-Registers, Pin diagram, I/O ports functions, Internal Memory organization, External Memory (ROM & RAM) interfacing

Module 2

8051 Instruction Set :

Addressing Modes, Data Transfer instructions, Arithmetic instructions, Logical instructions, Branch instructions, Bit manipulation instructions, Simple Assembly language program examples (without loops) to use these instructions

Module 3

8051 Stack, I/O Port Interfacing and Programming :

8051 Stack, Stack and Subroutine instructions, Assembly language program examples on subroutine and involving loops, Interfacing simple switch and LED to I/O ports to switch on/off LED with respect to switch status

Module 4

8051 Timers and Serial Port :

8051 Timers and Counters – Operation and Assembly language programming to generate a pulse using Mode-1 and a square wave using Mode-2 on a port pin, 8051 Serial Communication- Basics of Serial Data Communication, RS-232 standard, 9 pin RS232 signals, Simple Serial Port programming in Assembly and C to transmit a message and to receive data serially

Module 5

8051 Interrupts and Interfacing Applications :

8051 Interrupts, 8051 Assembly language programming to generate an external interrupt using a switch, 8051 C programming to generate a square waveform on a port pin using a Timer interrupt, Interfacing 8051 to ADC-0804, DAC, LCD and Stepper motor and their 8051 Assembly language interfacing programming

6 . Course Information

6 . 1 . 2 Text Books and Reference Books

TEXT BOOKS :

1 . "The 8051 Microcontroller and Embedded Systems – using assembly and C", Muhammad Ali Mazidi and Janice Gillespie Mazidi and Rollin D. McKinlay; PHI, 2006 / Pearson, 2006.

2 . "The 8051 Microcontroller", Kenneth J. Ayala, 3rd Edition, Thomson/Cengage Learning.

REFERENCE BOOKS :

1 . "The 8051 Microcontroller Based Embedded Systems", Manish K Patel, McGraw Hill, 2014, ISBN: 978-93-329-0125-4.

2 . "Microcontrollers: Architecture, Programming, Interfacing and System Design", Raj Kamal, Pearson Education, 2005.

HOD

6 . Course Information

6 . 2

Semester : 4 **Section :** B **Course :** MICROCONTROLLER

Period	Planned			Execution		
	Date	Topic	Source material to be referred	Date	Topic	Source material to be referred
			1			
1	2022-05-24	Microprocessor Vs Microcontroller	Text 1, Text 2, Ref 1,	2022-05-24	Microprocessor Vs Microcontroller	Text 1, Text 2, Ref 1,
2	2022-05-26	Embedded Systems	Text 2	2022-05-26	Embedded Systems	Text 2
3	2022-05-27	Embedded Microcontrollers	Text 1	2022-05-27	Embedded Microcontrollers	Text 1
4	2022-05-30	8051 Architecture-Registers	Text 1, Text 2, Ref 1,	2022-05-30	8051 Architecture-Registers	Text 1, Text 2, Ref 1,
5	2022-05-31	8051 Architecture-Registers	Text 1, Text 2, Ref 1,	2022-05-31	8051 Architecture-Registers	Text 1, Text 2, Ref 1,
6	2022-06-02	Pin diagram	Text 1, Text 2, Ref 1,	2022-06-02	Pin diagram	Text 1, Text 2, Ref 1,
7	2022-06-03	I/O ports functions	Text 1, Text 2, Ref 1,	2022-06-03	I/O ports functions	Text 1, Text 2, Ref 1,
8	2022-06-06	Internal Memory organization	Text 1, Text 2, Ref 1,	2022-06-06	Internal Memory organization	Text 1, Text 2, Ref 1,
9	2022-06-07	Internal Memory organization	Text 1, Text 2, Ref 1,	2022-06-07	Internal Memory organization	Text 1, Text 2, Ref 1,
10	2022-06-09	External Memory (ROM & RAM) interfacing	Text 1, Text 2, Ref 1,	2022-06-09	External Memory (ROM & RAM) interfacing	Text 1, Text 2, Ref 1,
			2			
11	2022-06-10	Addressing Modes	Text 1, Text 2, Ref 1,	2022-06-10	Addressing Modes	Text 1, Text 2, Ref 1,
12	2022-06-13	Addressing Modes		2022-06-13	Addressing Modes	Text 1, Ref 1, Ref 2,
13	2022-06-14	Data Transfer instructions	Text 1, Text 2, Ref 1,	2022-06-14	Data Transfer instructions	Text 1, Text 2, Ref 1,

14	2022-06-16	Arithmetic instructions	Text 1, Text 2, Ref 1,	2022-06-16	Arithmetic instructions	Text 1, Text 2, Ref 1,
15	2022-06-17	Arithmetic instructions	Text 1, Text 2, Ref 1,	2022-06-17	Arithmetic instructions	Text 1, Text 2, Ref 1,
16	2022-06-20	Logical instructions	Text 1, Text 2, Ref 1,	2022-06-20	Logical instructions	Text 1, Text 2, Ref 1,
17	2022-06-21	Logical instructions, Branch instructions	Text 1, Text 2,	2022-06-21	Logical instructions, Branch instructions	Text 1, Text 2,
18	2022-06-23	Branch instructions, Bit manipulation instructions	Text 1, Text 2, Ref 1,	2022-06-23	Branch instructions, Bit manipulation instructions	Text 1, Text 2, Ref 1,
19	2022-06-24	Bit manipulation instructions	Text 1, Text 2, Ref 1,	2022-06-24	Bit manipulation instructions	Text 1, Text 2, Ref 1,
20	2022-06-27	Simple Assembly language program examples (without loops) to use these instructions	Text 1, Text 2, Ref 1,	2022-06-27	Simple Assembly language program examples (without loops) to use these instructions	Text 1, Text 2, Ref 1,
			3			
21	2022-06-28	8051 Stack	Text 1, Text 2, Ref 1,	2022-06-28	8051 Stack	Text 1, Text 2, Ref 1,
22	2022-06-30	8051 Stack	Text 1, Text 2,	2022-06-30	8051 Stack	Text 1, Text 2,
23	2022-07-01	Stack and Subroutine instructions	Text 1, Text 2, Ref 1,	2022-07-01	Stack and Subroutine instructions	Text 1, Text 2, Ref 1,
24	2022-07-04	Stack and Subroutine instructions	Text 1, Text 2, Ref 1,	2022-07-04	Stack and Subroutine instructions	Text 1, Text 2, Ref 1,
25	2022-07-05	Assembly language program examples on subroutine and involving loops	Text 1, Text 2,	2022-07-05	Assembly language program examples on subroutine and involving loops	Text 1, Text 2,
26	2022-07-07	Assembly language program examples on subroutine and involving loops	Text 1	2022-07-07	Assembly language program examples on subroutine and involving loops	Text 1
27	2022-07-08	Assembly language program examples on subroutine and involving loops	Text 1, Text 2, Ref 1,	2022-07-08	Assembly language program examples on subroutine and involving loops	Text 1, Text 2, Ref 1,
28	2022-07-11	Assembly language program examples on subroutine and involving loops	Text 2, Text 1, Ref 1,	2022-07-11	Assembly language program examples on subroutine and involving loops	Text 2, Text 1, Ref 1,

29	2022-07-12	Interfacing simple switch and LED to I/O ports to switch on/off LED with respect to switch status	Text 1, Text 2, Ref 1,	2022-07-12	Interfacing simple switch and LED to I/O ports to switch on/off LED with respect to switch status	Text 1, Text 2, Ref 1,
30	2022-07-14	Interfacing simple switch and LED to I/O ports to switch on/off LED with respect to switch status	Text 1, Text 2, Ref 1,	2022-07-14	Interfacing simple switch and LED to I/O ports to switch on/off LED with respect to switch status	Text 1, Text 2, Ref 1,
			4			
31	2022-07-15	8051 Timers and Counters – Operation and Assembly language programming to generate a pulse using Mode-1 and a square wave using Mode-2 on a port pin	Text 1, Text 2, Ref 1,	2022-07-15	8051 Timers and Counters – Operation and Assembly language programming to generate a pulse using Mode-1 and a square wave using Mode-2 on a port pin	Text 1, Text 2, Ref 1,
32	2022-07-18	8051 Timers and Counters – Operation and Assembly language programming to generate a pulse using Mode-1 and a square wave using Mode-2 on a port pin	Text 1, Text 2, Ref 1,	2022-07-18	8051 Timers and Counters – Operation and Assembly language programming to generate a pulse using Mode-1 and a square wave using Mode-2 on a port pin	Text 1, Text 2, Ref 1,
33	2022-07-19	8051 Timers and Counters – Operation and Assembly language programming to generate a pulse using Mode-1 and a square wave using Mode-2 on a port pin	Text 1, Text 2, Ref 1,	2022-07-19	8051 Timers and Counters – Operation and Assembly language programming to generate a pulse using Mode-1 and a square wave using Mode-2 on a port pin	Text 1, Text 2, Ref 1,
34	2022-07-21	8051 Serial Communication- Basics of Serial Data Communication	Text 1, Text 2, Ref 1,	2022-07-21	8051 Serial Communication- Basics of Serial Data Communication	Text 1, Text 2, Ref 1,
35	2022-07-22	8051 Serial Communication- Basics of Serial Data Communication	Text 1, Text 2, Ref 1,	2022-07-22	8051 Serial Communication- Basics of Serial Data Communication	Text 1, Text 2, Ref 1,
36	2022-07-25	RS-232 standard	Text 1, Text 2, Ref 1,	2022-07-25	RS-232 standard	Text 1, Text 2, Ref 1,
37	2022-07-26	RS-232 standard, 9 pin RS232 signals	Text 1, Text 2, Ref 1,	2022-07-26	RS-232 standard, 9 pin RS232 signals	Text 1, Text 2, Ref 1,
38	2022-07-28	9 pin RS232 signals	Text 1, Text 2, Ref 1,	2022-07-28	9 pin RS232 signals	Text 1, Text 2, Ref 1,
39	2022-07-29	Simple Serial Port programming in Assembly and C to transmit a message and to receive data serially	Text 1, Text 2,	2022-07-29	Simple Serial Port programming in Assembly and C to transmit a message and to receive data serially	Text 1, Text 2,
40	2022-08-01	Simple Serial Port programming in Assembly and C to transmit a message and to receive data serially	Text 1, Text 2,	2022-08-01	Simple Serial Port programming in Assembly and C to transmit a message and to receive data serially	Text 1, Text 2,

5						
41	2022-08-02	8051 Interrupts	Text 1, Text 2, Ref 1,	2022-08-02	8051 Interrupts	Text 1, Text 2, Ref 1,
42	2022-08-04	8051 Interrupts	Text 1, Text 2, Ref 1,	2022-08-04	8051 Interrupts	Text 1, Text 2, Ref 1,
43	2022-08-05	8051 Assembly language programming to generate an external interrupt using a switch	Text 1, Text 2, Ref 1,	2022-08-05	8051 Assembly language programming to generate an external interrupt using a switch	Text 1, Text 2, Ref 1,
44	2022-08-08	8051 Assembly language programming to generate an external interrupt using a switch	Text 1, Text 2, Ref 1,	2022-08-08	8051 Assembly language programming to generate an external interrupt using a switch	Text 1, Text 2, Ref 1,
45	2022-08-11	8051 C programming to generate a square waveform on a port pin using a Timer interrupt	Text 1, Text 2,	2022-08-11	8051 C programming to generate a square waveform on a port pin using a Timer interrupt	Text 1, Text 2,
46	2022-08-12	8051 C programming to generate a square waveform on a port pin using a Timer interrupt	Text 1, Text 2,	2022-08-12	8051 C programming to generate a square waveform on a port pin using a Timer interrupt	Text 1, Text 2,
47	2022-08-16	Interfacing 8051 to ADC-0804	Text 1, Text 2,	2022-08-16	Interfacing 8051 to ADC-0804	Text 1, Text 2,
48	2022-08-18	Interfacing 8051 to ADC-0804	Text 1, Text 2,	2022-08-18	Interfacing 8051 to ADC-0804	Text 1, Text 2,
49	2022-08-19	DAC	Text 1, Text 2, Ref 1,	2022-08-19	DAC	Text 1, Text 2, Ref 1,
50	2022-08-22	LCD and Stepper motor and their 8051 Assembly language interfacing programming	Text 1, Text 2,	2022-08-22	LCD and Stepper motor and their 8051 Assembly language interfacing programming	Text 1, Text 2,

6 . Course Information

6 . 2 . 1 Compliance Report

Semester : 4 **Section :** B **Course :** MICROCONTROLLER

Module No.	# of Classes Planned(till date)	Planned Effort(till date)	# of Classes Executed(till date)	Actual Efforts(till date)	% Coverage
1	10	10hrs 0min	10	10hrs 0min	100.0
2	10	10hrs 0min	10	10hrs 0min	100.0
3	10	10hrs 0min	10	10hrs 0min	100.0
4	10	10hrs 0min	10	10hrs 0min	100.0
5	10	10hrs 0min	10	10hrs 0min	100.0

HOD

6 . Course Information

6 . 2 . 2 CO PO Mapping

Slight (Low) = 1 , Moderate (Medium) = 2 , Substantial (High) = 3 .

CO/ PO	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12
CO 1	2	1	1									
CO 2	2	2	1									
CO 3	2	2	1									
CO 4	2	2	2									

HOD

6 . Course Information

6 . 2 . 3 CO-PSO Mapping

Slight (Low) - 1 , Moderate (Medium) - 2 , Substantial (High) - 3

CO/PSO	PSO 1	PSO 2
CO 1	3	
CO 2	3	1
CO 3	3	1
CO 4	3	1

HOD

6 . Course Information

6 . 3 Other Assessment

ASSIGNMENT : 1

Semester:4-CBCS 2018

Subject : MICROCONTROLLER (18EC46)

Faculty : Divya

Max Marks: 10

Answer All Questions			
Q.No			**Max Marks**
1		*Explain with neat diagram, the programming model of 8051 Microcontroller (MC). Describe the function of various pins of 8051 Microcontroller with pin diagram. Explain with the help of diagram how to interface ROM and RAM to 8051 MC. Explain the difference between the following instructions (i) JNC and JNZ (ii) RRC A and RR A Explain the difference between SJMP, AJMP and LJMP. Interface 8 switches to port1 and 8 LEDs to port 0 and write a program to input the switch status and display on LEDs. Interface to 8051 i) Two switches sw1 & sw2 to port pins p2.0 & p2.1 ii) One LED to p1.0 and write ALP to realize 2 input XOR operation. Write an ALP with proper logical comments, to generate a square wave of frequency 2 kHz, on port pin P1.0 (LSB of port1). Use timer 0 in mode 2 (8 bit auto reload mode). Assume crystal =11.0592 MHz. Write a C program that continuously gets a single bit of data from P1.7 and sends*	10

Evaluation

USN	Name	Present (P) / Absent (Ab)	IA Total
4AI20EC057	Nirupam Hegde M P	P	9
4AI20EC058	Nisarga S	P	10
4AI20EC059	Nisarga Kanth K L	P	10
4AI20EC060	Nischitha C V	P	10
4AI20EC061	Nischitha H S	P	10
4AI20EC062	Nithin H M	P	10
4AI20EC063	Nithin N	P	10

USN	Name	Present (P) / Absent (Ab)	IA Total
4AI20EC064	Sai Geethika P V	P	10
4AI20EC065	Pallavi S	P	10
4AI20EC066	Pooja Manjunath Naik	P	10
4AI20EC067	Poojashree M N	P	10
4AI20EC068	Pragathi S	P	10
4AI20EC069	Prajwal S L	P	10
4AI20EC070	Praneetha K	P	10
4AI20EC071	Preksha C Y	P	10
4AI20EC072	Prathik R	P	10
4AI20EC073	Rahul B N	P	10
4AI20EC074	Rakshith K	P	0
4AI20EC075	Rakshith N P	P	9
4AI20EC076	Rudresh L S	P	10
4AI20EC077	Unnathi S V	P	10
4AI20EC078	Safa Ali	P	10
4AI20EC080	Sanmathi H M	P	10
4AI20EC081	Shabaz Khan	P	10
4AI20EC082	Shakthi B S	P	10
4AI20EC083	Sheethal M	P	10
4AI20EC084	Shree Sameehana R	P	10
4AI20EC085	Shree Vishnu N V	P	10
4AI20EC086	Shreya B M	P	10
4AI20EC087	Shwetha H S	P	10
4AI20EC088	Sneha N S	P	10
4AI20EC089	Sonika H P	P	10
4AI20EC090	Spoorthi D N	P	10
4AI20EC091	Srujan K J	P	10
4AI20EC092	Srusti B A	P	10

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USN	Name	Present (P) / Absent (Ab)	IA Total
4AI20EC093	Sudeep K P	P	10
4AI20EC094	Sugam Ganesh K S	P	10
4AI20EC095	Sugam K N	P	10
4AI20EC096	Sujay Urs C B	P	10
4AI20EC097	Sukhi D	P	10
4AI20EC098	Swamy Kotresh B	P	10
4AI20EC099	Swarna Gowri K S	P	10
4AI20EC100	Swathi B P	P	10
4AI20EC101	Swathisha H Shetty	P	10
4AI20EC102	Vagdevi M K	P	10
4AI20EC103	Vaishnavi S R	P	10
4AI20EC104	Varsha C J	P	10
4AI20EC105	Varshini S	P	10
4AI20EC106	Varshith D N	P	10
4AI20EC107	Varshitha S V	P	10
4AI20EC108	Vedhashree C R	P	10
4AI20EC109	Vinayak Bhyresh Onimani	P	0
4AI20EC110	Vinayaka M S	P	10
4AI20EC111	Vivek S M	P	10
4AI20EC112	Yashwanth K N	P	10
4AI20EC113	Yogish N S	P	10
4AI21EC402	Nandashree A G	P	10
4AI21EC403	Sahana K R	P	10

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6 . Course Information

6 . 4 Internal Assessment

Internal : 1

Semester:4-CBCS 2018 | Date : 03/07/2022

Subject : MICROCONTROLLER (18EC46) | Time : 12:00 - 13:00

Faculty : Divya | Max Marks: 50

Answer Any 2 Questions					
Q.No			Max Marks	CO	BT/ CL
1a		*List the specific features of 8051 with the help of neat block diagram*	10	1	L1
1b		*Explain the function of PORT 0 with neat diagram*	10	1	L2

1c		*Distinguish between Microprocessor and Microcontroller*	5	1	L2
		OR			
2a		*Explain the organization of internal memory in 8051*	10	1	L1
2b		*Interface 8051 to external ROM (8K) and RAM (4K) and explain how 8051 access them*	10	1	L2

2c		*Explain 8051 crystal oscillator and clock with waveforms.*	5	1	L2
3a		*Explain different addressing modes of 8051.Give an example for each of them.*	12	2	L2
3b		*(i)Explain bit pattern of Program status word* *(ii) Explain Program counter and data pointer*	13	1	L2
		OR			

2c		*Explain 8051 crystal oscillator and clock with waveforms.*	5	1	L2
3a		*Explain different addressing modes of 8051.Give an example for each of them.*	12	2	L2
3b		*(i)Explain bit pattern of Program status word* *(ii) Explain Program counter and data pointer*	13	1	L2
		OR			

4a		*(i)Write ALP with proper logical comments to clear 8 RAM locations starting at RAM address 50H* *(ii)Write the stack and stack pointer contents after the execution of each of the following instructions* *MOV R7,#52H* *MOV R2,#20H* *MOV R0, #14H* *PUSH 02H* *PUSH 00H* *PUSH 07H* *POP 04H* *POP 05H* *POP 03H*	12	2	L2
4b		*Explain the function of various pins of 8051 with neat diagram*	13	1	L2

Evaluation

USN	Name	Present (P) / Absent (Ab)	Q1			Q2			Q3		Q4		IA Total	BT/CL
			a	b	c	a	b	c	a	b	a	b		
4AI20EC057	Nirupam Hegde M P	P	0	0	0	0	0	0	0	0	0	0	0	No Level
4AI20EC058	Nisarga S	P	8	8	5	0	0	0	6	7	0	0	34	Understand
4AI20EC059	Nisarga Kanth K L	P	6	8	4	0	0	0	7	5	0	0	30	Understand
4AI20EC060	Nischitha C V	P	9	5	5	0	0	0	2	2	0	0	23	Understand
4AI20EC061	Nischitha H S	P	8	7	4	0	0	0	7	0	0	0	26	Understand
4AI20EC062	Nithin H M	P	9	6	5	0	0	0	12	5	0	0	37	Understand
4AI20EC063	Nithin N	P	7	0	0	0	0	0	11	0	0	0	18	Understand
4AI20EC064	Sai Geethika P V	P	8	7	5	0	0	0	12	10	0	0	42	Understand
4AI20EC065	Pallavi S	P	1	0	0	0	0	0	1	8	0	0	10	Understand
4AI20EC066	Pooja Manjunath Naik	P	5	8	5	0	0	0	9	11	0	0	38	Understand

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USN	Name	Present (P) / Absent (Ab)	Q1			Q2			Q3		Q4		IA Total	BT/CL
			a	b	c	a	b	c	a	b	a	b		
4AI20EC067	Poojashree M N	P	9	6	5	0	0	0	3	6	0	0	29	Understand
4AI20EC068	Pragathi S	P	8	9	5	0	0	0	7	11	0	0	40	Understand
4AI20EC069	Prajwal S L	P	0	0	5	0	0	0	0	0	0	0	5	Understand
4AI20EC070	Praneetha K	P	0	8	5	0	0	0	4	9	0	0	26	Understand
4AI20EC071	Preksha C Y	P	0	0	0	0	0	0	0	0	0	0	0	No Level
4AI20EC072	Prathik R	P	3	5	5	0	0	0	0	0	0	0	13	Understand
4AI20EC073	Rahul B N	P	7	6	5	0	0	0	2	0	3	0	21	Understand
4AI20EC074	Rakshith K	P	6	0	5	0	0	0	0	0	0	0	11	Understand
4AI20EC075	Rakshith N P	P	0	0	0	0	0	0	6	9	0	0	15	Understand
4AI20EC076	Rudresh L S	P	0	0	2	0	0	0	9	0	0	0	11	Understand
4AI20EC077	Unnathi S V	P	8	2	5	0	0	0	2	3	0	0	20	Understand
4AI20EC078	Safa Ali	P	7	4	3	0	0	0	0	0	3	2	19	Understand
4AI20EC080	Sanmathi H M	P	5	0	5	0	0	0	1	0	0	8	18	Understand
4AI20EC081	Shabaz Khan	P	8	3	4	0	0	0	2	4	0	0	21	Understand
4AI20EC082	Shakthi B S	P	2	4	3	0	0	0	2	0	0	0	11	Understand
4AI20EC083	Sheethal M	P	7	0	0	0	0	0	0	7	0	0	14	Understand
4AI20EC084	Shree Sameehana R	P	10	8	5	0	0	0	12	10	0	0	45	Understand
4AI20EC085	Shree Vishnu N V	P	4	5	4	0	0	0	12	3	0	0	28	Understand
4AI20EC086	Shreya B M	P	9	6	3	0	0	0	5	5	0	0	28	Understand
4AI20EC087	Shwetha H S	P	9	7	5	0	0	0	9	11	0	0	41	Understand
4AI20EC088	Sneha N S	P	10	8	4	0	0	0	5	10	0	0	37	Understand
4AI20EC089	Sonika H P	P	5	4	1	0	0	0	0	0	0	4	14	Remember
4AI20EC090	Spoorthi D N	P	5	9	4	0	0	0	5	5	0	0	28	Understand
4AI20EC091	Srujan K J	P	0	0	2	0	0	0	7	0	0	0	9	Understand
4AI20EC092	Srusti B A	P	9	5	0	0	0	0	4	1	0	0	19	Understand
4AI20EC093	Sudeep K P	P	6	2	4	0	0	0	0	0	0	6	18	Understand
4AI20EC094	Sugam Ganesh K S	P	5	2	1	0	0	0	0	0	2	0	10	Remember
4AI20EC095	Sugam K N	P	10	0	5	0	0	0	1	0	0	0	16	Understand
4AI20EC096	Sujay Urs C B	P	8	0	0	0	0	0	4	0	0	0	12	Remember
4AI20EC097	Sukhi D	P	9	8	5	0	0	0	5	2	0	0	29	Understand
4AI20EC098	Swamy Kotresh B	P	4	0	4	3	0	0	2	4	0	0	14	Understand
4AI20EC099	Swarna Gowri K S	P	5	3	1	0	0	0	3	5	0	0	17	Remember
4AI20EC100	Swathi B P	P	9	7	5	0	0	0	10	12	0	0	43	Understand
4AI20EC101	Swathisha H Shetty	P	8	2	1	0	0	0	3	3	0	0	17	Remember
4AI20EC102	Vagdevi M K	P	0	2	2	0	0	0	0	0	0	0	4	No Level
4AI20EC103	Vaishnavi S R	P	9	9	5	0	0	0	10	9	0	0	42	Understand

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USN	Name	Present (P) / Absent (Ab)	Q1			Q2			Q3		Q4		IA Total	BT/CL
			a	b	c	a	b	c	a	b	a	b		
4AI20EC104	Varsha C J	P	8	5	5	0	0	0	3	0	0	0	21	Understand
4AI20EC105	Varshini S	P	3	2	2	0	0	0	5	0	3	0	12	No Level
4AI20EC106	Varshith D N	P	6	8	0	0	0	0	10	0	0	0	24	Understand
4AI20EC107	Varshitha S V	P	7	8	5	0	0	0	9	9	0	0	38	Understand
4AI20EC108	Vedhashree C R	P	8	0	5	0	0	0	2	2	0	0	17	Understand
4AI20EC109	Vinayak Bhyresh Onimani	P	9	2	5	0	0	0	10	5	0	0	31	Understand
4AI20EC110	Vinayaka M S	P	10	0	5	0	0	0	8	4	0	0	27	Understand
4AI20EC111	Vivek S M	P	10	10	5	0	0	0	11	10	0	0	46	Understand
4AI20EC112	Yashwanth K N	P	8	0	5	0	0	0	8	8	0	0	29	Understand
4AI20EC113	Yogish N S	P	4	4	0	0	0	0	1	0	0	0	9	No Level
4AI21EC402	Nandashree A G	P	8	0	5	0	0	0	4	5	0	4	22	Understand
4AI21EC403	Sahana K R	P	4	2	1	0	0	0	0	0	0	2	9	No Level

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2 Scheme of Evaluation

Date: 03/07/2022
Test: 1
Time 12-1 PM
Marks: 50

AIT, E&C Dept

Sub: 8051 Microcontrollers (18EC46)

Answer one full question from each part

Q. No		PART A	CO	BT/ CL	marks
1	a	**List the specific features of 8051 with the help of neat block diagram.**	CO1	L1	10

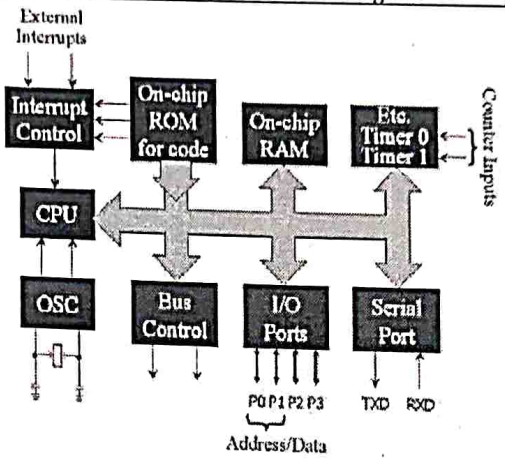


FIGURE - 4M

Salient features of 8051 microcontroller are given below.

- Eight bit CPU
- On chip clock oscillator
- 4Kbytes of internal program memory (code memory) [ROM]
- 128 bytes of internal data memory [RAM]
- 64 Kbytes of external program memory address space.
- 64 Kbytes of external data memory address space.
- 32 bi directional I/O lines (can be used as four 8 bit ports or 32 individually addressable I/O lines)
- Two 16 Bit Timer/Counter :T0, T1
- Full Duplex serial data receiver/transmitter
- Four Register banks with 8 registers in each bank.
- Sixteen bit Program counter (PC) and a data pointer (DPTR)
- 8 Bit Program Status Word (PSW)
- 8 Bit Stack Pointer
- Five vector interrupt structure (RESET not considered as an interrupt.)
- 8051 CPU consists of 8 bit ALU with associated registers like accumulator 'A', B register, PSW,SP, 16 bit program counter, stack pointer.
- ALU can perform arithmetic and logic functions on 8 bit variables.
- 8051 has 128 bytes of internal RAM which is divided into
  - Working registers [00 – 1F]
  - Bit addressable memory area [20 – 2F]
  - General purpose memory area (Scratch pad memory) [30-7F]

EXPLANATION - 6M

	b	**Explain the function of PORT 0 with neat diagram** ▪ can be used as input or output. ▪ **also designated as AD0-AD7,** allowing it to be used for both address and data when	CO1	L2	10

connected to an external memory.

- When control is '1', the port is used for address/data interfacing.
- When the control is '0', the port can be used as a normal bidirectional I/O port.
- 8051 multiplexes address and data through Port 0 to save pins.
- ALE indicates if P0 has address or data
  - When ALE = 0, it provides data D0-D7
  - When ALE = 1, it has address A0-A7

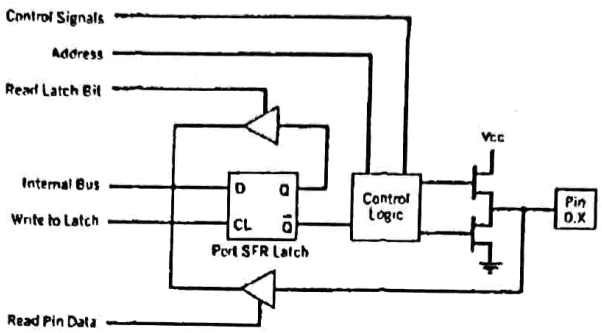


FIGURE - 4M

EXPLANATION - 6M

PORT 0 STRUCTURE

when a pin is to be used as an input, a 1 *must be* written to the corresponding port 0 latch by the program, thus turning both of the output transistors off, which in turn causes the pin to "float" in a high-impedance state, and the pin is essentially connected to the input buffer.

When used as an output, the pin latches that are programmed to a 0 will turn on the lower FET, grounding the pin. All latches that are programmed to a 1 still float; thus, external pullup resistors will be needed to supply a logic high when using port 0 as an output.

When port 0 is used as an address bus to external memory, internal control signals switch the address lines to the gates of the Field Effect Transistories (FETs). A logic 1 on an address bit will turn the upper FET on and the lower FET off to provide a logic high at the pin. When the address bit is a zero, the lower FET is on and the upper FET off to provide a logic low at the pin. After the address has been formed and latched into external circuits by the Address Latch Enable (ALE) pulse, the bus is turned around to become a data bus. Port 0 now reads data from the external memory and must be configured as an input, so a logic 1 is automatically written by internal control logic to all port 0 latches.

c	Distinguish between Microprocessor and Microcontroller	CO1	L2	05

MINIMUM 5 DIFFERENCES - 5M

Microprocessor	Microcontroller
Microprocessor contains ALU, General purpose registers, stack pointer, program counter, clock timing circuit, interrupt circuit	Microcontroller contains the circuitry of microprocessor, and in addition it has built in ROM, RAM, I/O Devices, Timers/Counters etc.
It has many instructions to move data between memory and CPU	It has few instructions to move data between memory and CPU

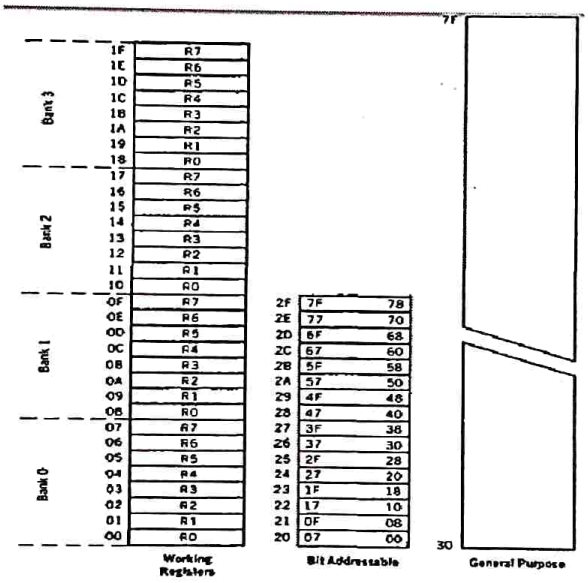
		Few bit handling instruction	It has many bit handling instructions	
		Less number of pins are multifunctional	More number of pins are multifunctional	
		Single memory map for data and code (program)	Separate memory map for data and code (program)	
		Access time for memory and IO are more	Less access time for built in memory and IO.	
		Microprocessor based system requires additional hardware	It requires less additional hardware	
		More flexible in the design point of view	Less flexible since the additional circuits which is residing inside the microcontroller is fixed for a particular microcontroller	
		Large number of instructions with flexible addressing modes	Limited number of instructions with few addressing modes	

		OR			
2	a	**Explain the organization of internal memory in 8051.**	CO1	L1	10

- **On-chip memory organized into 2 categories:**

i. **Internal RAM**

ii. **Internal ROM**



Internal RAM

- **Thirty-two bytes from address 00h to 1Fh that make up 32 working registers** organized as fourbanks of eight registers each. (Bank0- Bank3; with each bank having registers R0-R7)
- **Each register can be addressed by name** (when its bank is selected) **or by its RAM address.**
- **Thus R0 of bank 3 is R0** (if bank 3 is currently selected) or address 18h (whether bank 3 is selectedor not).
- **Bits RS0 and RS1 in the PSW determine** which bank of registers is currently in use.
- Register banks not selected can be used as general-purpose RAM.
  - **Bank 0 is selected upon reset.**

- A *bit-addressable* area of 16 bytes occupies RAM *byte* addresses 20h to 2Fh, forming a total of 128 addressable bits.
- An addressable bit may be specified by its *bit* address of 00h to 7Fh, or 8 bits may form any *byte* address from 20h to 2Fh.
  - Thus, for example, bit address 4Fh is also bit 7 of byte address 29h.
  - Addressable bits are useful when the program need only remember a binary event (switchon, light off, etc.).
- A general-purpose RAM area above the bit area, from 30h to 7Fh, addressable as bytes.
- Special Function Registers are used to program and control different on-chip hardware peripherals like Timers, Serial Port, I/O Ports etc.
- The address space from 80H to FFH is allocated to SFRs.
- Only 21 locations are assigned to SFRs.
- Each SFR has one Byte Address and also a unique name which specifies its purpose. Some SFRs are bit addressable

Internal ROM

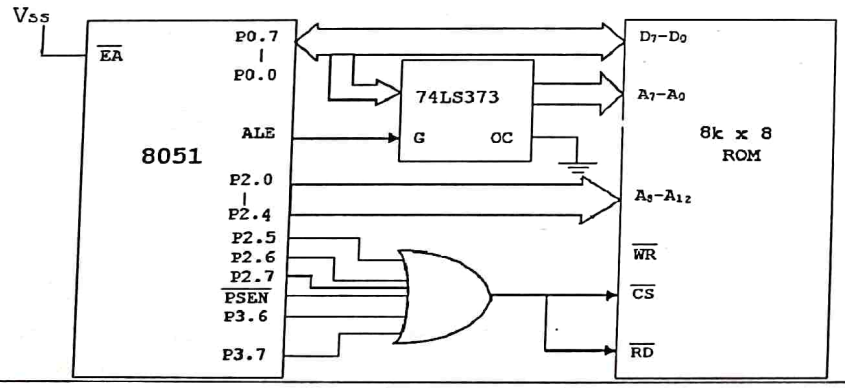
- The 8051 is organized so that data memory and program code memory can be in **two entirely different physical memory entities; *each* has the same address ranges.**
- A corresponding block of internal program code, contained in an internal ROM, occupies code address space 0000h to 0FFFh.
- The PC is ordinarily used to address program code bytes from addresses 0000h to 0FFFh.
- Program addresses higher than 0FFFh, which exceed the internal ROM capacity, will cause the 8051 to automatically fetch code bytes from external program memory.
- Code bytes can also be fetched exclusively from an external memory, addresses 0000h toFFFFh, by connecting the external access pin (EA pin 31 on the DIP) to ground.
- The PC does not care where the code is; the circuit designer decides whether the code is found totally in internal ROM, totally in external ROM, or in a combination of internal and externalROM.

FIGURE 3M EXPLANATION - 7M

b	Interface 8051 to external ROM (8K) and RAM (4K) and explain how 8051 access them.	CO1	L2	10

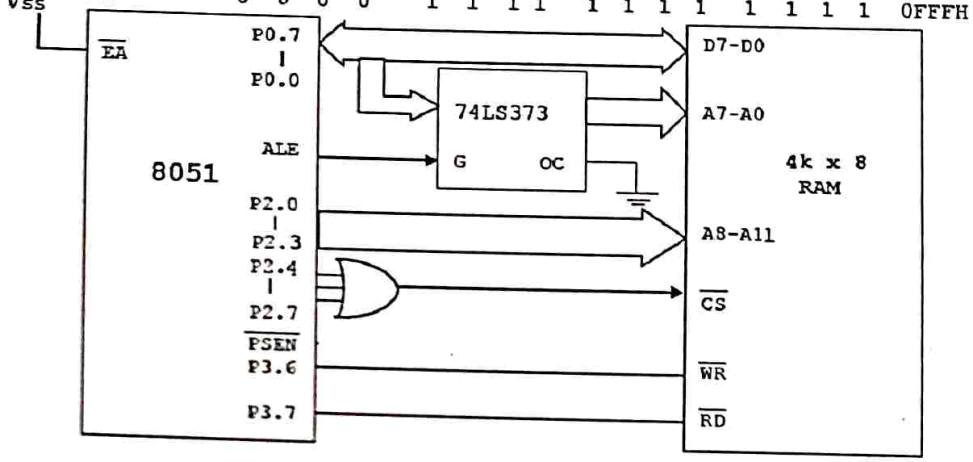
No. of address lines required for 8K ROM $2^n = 8K$. n=13. Hence address lines $A_0 - A_{12}$ are used.

Address	A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	HEX adrs.
starting	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000H
end	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1FFFH



No. of address lines required for 4K RAM $2^n = 4K$. n=12. Hence address lines $A_0 - A_{11}$ are used.

	A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	HEX adrs.
starting	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000H
end	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	0FFFH

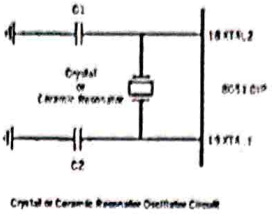


5M FOR EACH DESIGN

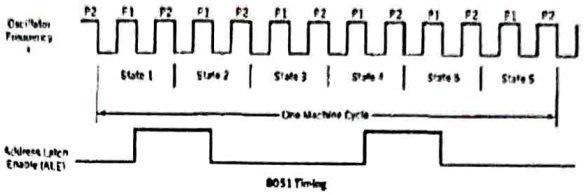
c | Explain 8051 crystal oscillator and clock with waveforms. | CO1 | L2 | 05

➢ The heart of the 8051 is the circuitry that generates the clock pulses by which all internal operations are synchronized.

- Pins XTAL1 and XTAL2 are provided for connecting a resonant network to form an oscillator.
- The 8051 requires an external oscillator circuit. The oscillator circuit usually runs around 12MHz. the crystal generates 12M pulses in one second. The pulse is used to synchronize the system operation in a controlled pace.
- A quartz crystal oscillator is connected to inputs XTAL1 (pin19) and XTAL2 (pin18)
- The crystal frequency is the basic internal clock frequency of the microcontroller.
- Manufacturers provide designs that run at max and min frequencies, typically 1MHz to 16MHz.
- The quartz crystal oscillator also needs two capacitors of 30pF value.
- The clock frequency f, establishes the smallest interval of time within the microcontroller, called the Pulse time P.
- The smallest time interval to execute any simple instruction or part of a complex instruction is called the MACHINE CYCLE.
- A machine cycle is made up of six states.
- A state is the basic time interval for discrete operations of the microcontroller such as fetching an opcode byte, decoding an opcode, executing an opcode or writing a data byte.



Crystal or Ceramic Resonator Oscillator Circuit



8051 Timing

- Two oscillator pulses define each state.
- Program instructions may require one, two or four machine cycles for execution, based on the type of instruction.
- Time required to execute any instruction is given by

$$Tinst = \frac{C \times 12d}{\text{crystal frequency}}$$

Where C = number of clock cycles, 12d means decimal number 12.

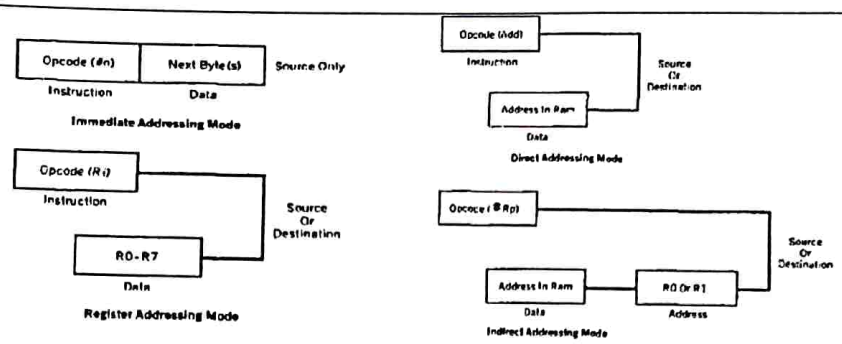
FIGURE - 2M EXPLANATION - 3M

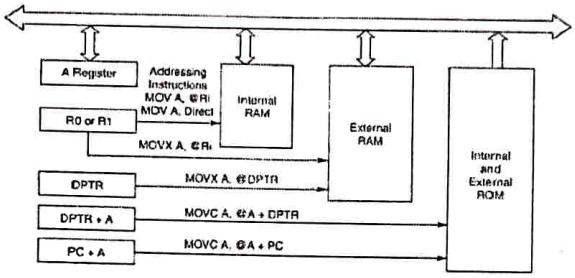
PART B

3	a	**Explain different addressing modes of 8051.Give an example for each of them.**	CO2	L2	12

The CPU can access data in various ways, which are called addressing modes In 8051there are 6 types of addressing modes:

1. Immediate Addressing mode
2. Register Addressing mode
3. Direct Addressing mode
4. Register Indirect Addressing mode
5. Indexed Addressing mode
6. Implied Addressing mode





6 ADDRESSING MODE WITH EXAMPLE – 2 M EACH X6 =

b	(i)Explain bit pattern of Program status word (ii) Explain Program counter and data pointer	CO1	L2	13

7	6	5	4	3	2	1	0
CY	AC	F0	RS1	RS0	OV	-	P

THE PROGRAM STATUS WORD (PSW) SPECIAL FUNCTION REGISTER

Bit	Symbol	Function
7	CY	Carry flag; used in arithmetic, JUMP, ROTATE, and BOOLEAN instructions
6	AC	Auxiliary carry flag; used for BCD arithmetic
5	F0	User flag 0
2	OV	Overflow flag; used in arithmetic instructions
1	-	Reserved for future use
0	P	Parity flag; shows parity of register A; 1 = Odd Parity

4	RS1	Register bank select bit 1
3	RS0	Register bank select bit 0

RS1	RS0	Function
0	0	Select register bank 0
0	1	Select register bank 1
1	0	Select register bank 2
1	1	Select register bank 3

PSW – 7M

Program Counter (PC) and Data Pointer (DPTR) - 3M EACH -3X2 = 6M

- Program instruction bytes are fetched from locations in memory that are addressed by the PC.
- The PC is automatically incremented after every instruction byte is fetched and may alsobe altered by certain instructions.
- The PC is the only register that does not have an internal address.
- The DPTR register is made up of two 8-bit registers, named DPH and DPL
- Are used to furnish memory addresses for internal and external code access and externaldata access.
- The DPTR is under the control of program instructions
- Can be specified by its 16-bit name, DPTR, or by each individual byte name, DPH and DPL.
- DPTR does not have a single internal address; DPH and DPL are each assigned an address.

OR

	a	**(i)Write ALP with proper logical comments to clear 8 RAM locations starting at RAM address 50H** **(ii)Write the stack and stack pointer contents after the execution of each of the following instructions** **MOV R7,#52H** **MOV R2,#20H** **MOV R0, #14H** **PUSH 02H** **PUSH 00H** **PUSH 07H** **POP 04H** **POP 05H** **POP 03H**	CO2	L2	12

(i) PROGRAM WITH COMMENTS - 6M

```
        ORG 0000H
        MOV R0, #50H   ; Initialize r0 with the address 50h
        MOV R1,#08H    ; Initialize R1 as a counter
        MOV A, #00H    ; Clear A
BACK :  MOV @R0, A     ; Copy A to address specified
        INC R0         ; Increment address pointer
        DJNZ R1, BACK  ; Decrement counter & if counter ≠0, then jump to label Back
HERE:   SJMP HERE
        END
```

ii) 3M FOR PUSH & 3M FOR POP OPERATION

```
MOV R7,#52H   ; R7 = 52H
MOV R2,#20H   ; R2 = 20H
MOV R0, #14H  ; R0 = 14H
PUSH 02H
PUSH 00H
PUSH 07H
```

BEFORE PUSH

0A		
09		
08		
07		TOS

AFTER PUSH 02H – Contents of R2 is copied to Stack and SP is incremented by 1

0A		
09		
08	20H	TOS
07		

AFTER PUSH 00H – Contents of R0 is copied to Stack and SP is incremented by 1

0A		
09	14H	TOS
08	20H	
07		

AFTER PUSH 07H – Contents of R7 is copied to Stack and SP is incremented by 1

0A	52H	TOS
09	14H	
08	20H	
07		

AFTER POP 04H – Contents from TOS is copied to register R4 and SP is decremented by 1

0A		
09	14H	TOS
08	20H	
07		

R4 = 52H

AFTER POP 05H – Contents from TOS is copied to register R5 and SP is decremented by 1

0A		
09		
08	20H	TOS
07		

R5 = 14H

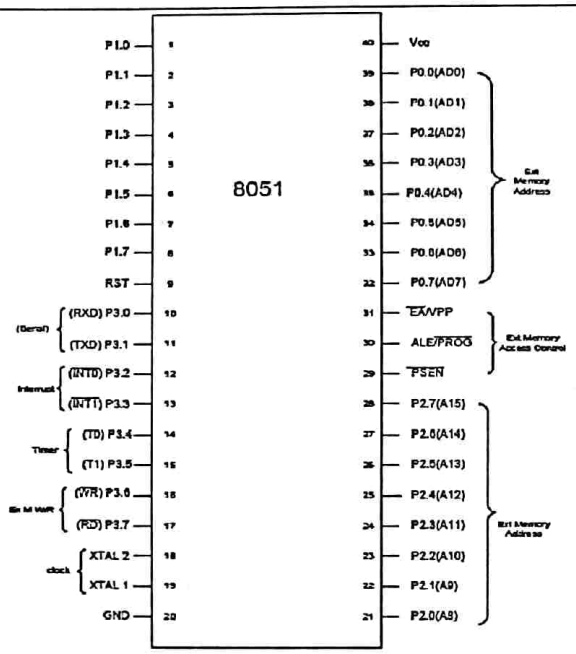
AFTER POP 03H – Contents from TOS is copied to register R3 and SP is decremented by 1

0A		
09		
08		
07		TOS

R3 = 20H

	b	Explain the function of various pins of 8051 with neat diagram	CO1	L2	13

PIN DIAGRAM – 5M
EXPLANATION OF PINS - 8M



Pins 1-8	PORT 1. Each of these pins can be configured as an input or an output.
Pin 9	RESET. A logic one on this pin disables the microcontroller and clears the contents of most registers. In other words, the positive voltage on this pin resets the microcontroller. By applying logic zero to this pin, the program starts execution from the beginning.
Pins10-17	PORT 3. Similar to port 1, each of these pins can serve as general input or output. Besides, all of them have alternative functions
Pin 10	RXD. Serial asynchronous communication input or Serial synchronous communication output.
Pin 11	TXD. Serial asynchronous communication output or Serial synchronous communication clock output.
Pin 12	INT0.External Interrupt 0 input
Pin 13	INT1. External Interrupt 1 input
Pin 14	T0. Counter 0 clock input
Pin 15	T1. Counter 1 clock input
Pin 16	WR. Write to external (additional) RAM
Pin 17	RD. Read from external RAM
Pin 18, 19	XTAL2, XTAL1. Internal oscillator input and output. A quartz crystal which specifies operating frequency is usually connected to these pins.
Pin 20	GND. Ground.

Pin 21-28	Port 2. If there is no intention to use external memory then these port pins are configured as general inputs/outputs. In case external memory is used, the higher address byte, i.e. addresses A8-A15 will appear on this port. Even though memory with capacity of 64Kb is not used, which means that not all eight port bits are used for its addressing, the rest of them are not available as inputs/outputs.
Pin 29	$\overline{PSEN}$ =PROGRAM STORE ENABLE, is an output pin used to activate external ROM. This pin is connected to OE (output enable) pin of the ROM. If external ROM is used for storing program then a logic zero (0) appears on it every time the microcontroller reads a byte from memory.
Pin 30	**ALE, "address latch enable"**, is an output pin and is active high • The 8051 multiplexes address and data through port 0 to save pins. • ALE pin is used for demultiplexing the address and data ▪ When ALE=0, P0 provides data D0-D7 ▪ When ALE=1, P0 has address A0-A7
Pin 31	$\overline{EA}$ - External Access, is an input pin, used for the selection of on-chip or off-chip ROM ➢ $\overline{EA}$ = 1,8051 reads program code from on-chip ROM • If program address is outside the range of on-chip ROM, then external ROM is accessed as shown in the figure below. ➢ $\overline{EA}$ = 1 , program code is read from external memory only, irrespective of on-chip ROM as shown in the figure below.
Pin 32-39	PORT 0. Similar to P2, if external memory is not used, these pins can be used as general inputs/outputs. Otherwise, P0 is configured as address output (A0- A7) when the ALE pin is driven high (1) or as data output (Data Bus) when the ALE pin is driven low (0).
Pin 40	VCC. +5V power supply.

@@@

Internal : 2

Semester:4-CBCS 2018 — Date : 02/08/2022

Subject : MICROCONTROLLER (18EC46) — Time : 12:00 - 13:00

Faculty : Divya — Max Marks: 50

Part A
Answer any 1 questions

Q.No			Max Marks	CO	BT/CL
1a		*Explain the following instructions with suitable examples: (i) DA A (ii) SWAP A (iii) XCHD A, SRC (iv) ANL A, R1 (v) SETB 00h*	10	2	L1
1b		*Write an assembly language program with proper logical comments to check whether the given byte is bitwise palindrome or not using subroutine. If palindrome store FFH otherwise store 00H.*	10	2	L2
1c		*Write an assembly language program with proper logical comments to add an array of six 8-bit numbers starting from address 9000H and store the result in 900AH.*	5	2	L2

4a		*Interface to 8051 i) Two switches sw1 & sw2 to port pins p2.0 & p2.1 ii) One LED to p1.0 and write ALP to realize 2 input XOR operation.*	10	4	L2
4b		*Write an assembly language program with proper logical comments to convert hexadecimal number to ASCII. Explain the program with suitable example.*	10	2	L2
4c		*A switch is connected to pin P1.7. Write a program to check the status of SW and perform the following: (a) If SW=0, send letter 'N' to P2 (b) If SW=1, send letter 'Y' to P2*	5	4	L2

2a		*Define subroutine and explain the instructions related to subroutine in 8051.*	10	2	L1
2b		*Write an assembly language program with proper logical comments to add 2 multibyte numbers using subroutine.*	10	2	L2
2c		*Explain the difference between the following mnemonics: (i) J NC and J NZ (ii) RRC A and RR A*	5	2	L2
Part B					
Answer any 1 questions					
Q.No			**Max Marks**	**CO**	**BT/CL**

3a		*Interface 8 switches to port1 and 8 LEDs to port 0 and write a program to input the switch status and display on LEDs.*	10	4	L2
3b		*Write an assembly language program with proper logical comments to find whether the data 7Fh is positive or negative. If positive store FFh in register R1 else store 00 at same location. Explain with suitable example.*	10	2	L2
3c		*Write a program to perform the following: (a) Keep monitoring the P1.2 bit until it becomes high (b) When P1.2 becomes high, write value 45H to port 0 (c) Send a high-to-low (H-to-L) pulse to P2.3*	5	4	L2

ADICHUNCHANAGIRI INSTITUTE OF TECHNOLOGY

Department of Electronics & Communication Engineering (EC)

USN	Name	Present (P) / Absent (Ab)	Q1			Q2			Q3			Q4			IA Total	BT/CL
			a	b	c	a	b	c	a	b	c	a	b	c		
4AI20EC091	Srujan K J	P	0	0	0	5	3	1	0	0	0	3	0	2	14	Remember
4AI20EC092	Srusti B A	P	3	9	0	0	0	0	0	0	0	0	6	3	21	Understand
4AI20EC093	Sudeep K P	P	0	0	0	8	6	1	0	0	0	7	6	3	31	Understand
4AI20EC094	Sugam Ganesh K S	P	0	0	0	0	5	1	0	0	0	0	5	2	13	Understand
4AI20EC095	Sugam K N	P	0	0	0	7	10	1	10	0	0	0	0	0	28	Understand
4AI20EC096	Sujay Urs C B	P	0	0	0	0	5	0	0	0	0	0	5	3	13	Understand
4AI20EC097	Sukhi D	P	5.5	8	3	0	0	0	0	0	0	0	9	3.5	29	Understand
4AI20EC098	Swamy Kotresh B	P	3	7	0	0	0	0	0	0	0	7	3	0	20	Understand
4AI20EC099	Swarna Gowri K S	P	3	7	0	7	9	1	0	0	4	0	0	0	21	Understand
4AI20EC100	Swathi B P	P	4	0	0	8	1	0	10	0	0	4	2	5	20	Understand
4AI20EC101	Swathisha H Shetty	P	0	0	0	6	6	1	0	0	0	6	5	2	26	Understand
4AI20EC102	Vagdevi M K	P	0	0	0	1	5	1	0	0	0	5	5	1	18	Understand
4AI20EC103	Vaishnavi S R	P	8	8	2	0	0	0	0	0	0	4	10	4	36	Understand
4AI20EC104	Varsha C J	P	5.5	5.5	0	0	0	0	0	0	0	0	10	2	23	Understand
4AI20EC105	Varshini S	P	2	5	0	0	0	0	0	0	1	2	0	3	12	Understand
4AI20EC106	Varshith D N	P	0	0	0	10	9	2	0	0	0	0	7	4	32	Understand
4AI20EC107	Varshitha S V	P	0	0	0	5	6.5	3.5	7	0	0	2	3	4	24	Understand
4AI20EC108	Vedhashree C R	P	4	9	0	0	0	0	0	0	0	10	7	2	32	Understand
4AI20EC109	Vinayak Bhyresh Onimani	P	0	0	0	4	2	4	0	0	0	0	0	1	11	Understand
4AI20EC110	Vinayaka M S	P	0	0	0	4	6	0	0	0	0	0	7	3	20	Understand
4AI20EC111	Vivek S M	P	10	10	5	0	0	0	0	0	0	8	8	5	46	Understand
4AI20EC112	Yashwanth K N	P	0	0	0	5	0	3	10	0	5	0	0	0	23	Understand
4AI20EC113	Yogish N S	P	0	0	0	0	6	0	8	0	0	0	6	0	14	Understand
4AI21EC402	Nandashree A G	P	4	9	0	0	0	0	0	0	0	10	7	4	34	Understand
4AI21EC403	Sahana K R	P	3	7	0	0	0	0	0	0	0	4	4	2	20	Understand

Evaluation

USN	Name	Present (P) / Absent (Ab)	Q1			Q2			Q3			Q4			IA Total	BT/CL
			a	b	c	a	b	c	a	b	c	a	b	c		
4AI20EC057	Nirupam Hegde M P	P	0	0	0	6	5	0	0	0	0	5	6	3	25	Understand
4AI20EC058	Nisarga S	P	5.5	9	2.5	0	0	0	10	7	4	0	0	0	38	Understand
4AI20EC059	Nisarga Kanth K L	P	4	0	0	1	2	0	0	0	0	4	0	0	8	No Level
4AI20EC060	Nischitha C V	P	4	8	0	0	0	0	0	0	0	4	7	5	28	Understand
4AI20EC061	Nischitha H S	P	4	8	1	0	0	0	0	0	0	9	6	5	33	Understand
4AI20EC062	Nithin H M	P	0	0	0	10	10	4	0	0	0	6	7	4	41	Understand
4AI20EC063	Nithin N	P	0	0	0	0	5	0	0	0	0	0	5	2	12	Understand
4AI20EC064	Sai Geethika P V	P	9	7	4	0	0	0	9	9	4	0	0	0	42	Understand
4AI20EC065	Pallavi S	P	0	0	0	6	0	0	0	0	0	8	6	4	24	Understand
4AI20EC066	Pooja Manjunath Naik	P	0	0	0	6	9	3	0	0	0	8	9	5	40	Understand
4AI20EC067	Poojashree M N	P	0	0	0	5	8	1	0	0	0	3	4	3	24	Understand
4AI20EC068	Pragathi S	P	0	0	0	4	10	4	0	0	0	2	8	4	32	Understand
4AI20EC069	Prajwal S L	P	0	0	0	0	8	1	0	0	0	0	4	5	18	Understand
4AI20EC070	Praneetha K	P	0	0	0	9	9	4	0	0	0	7	8	4	41	Understand
4AI20EC071	Preksha C Y	P	2	0	1	0	0	0	7	0	0	4	0	0	10	Understand
4AI20EC072	Prathik R	P	0	5	0	0	0	0	5	5	0	0	5	5	15	Understand
4AI20EC073	Rahul B N	P	6	10	0	0	0	0	0	0	0	6	5	5	32	Understand
4AI20EC074	Rakshith K	P	0	5	0	0	0	0	0	0	0	0	5	0	10	Understand
4AI20EC075	Rakshith N P	P	0	0	0	0	0	0	0	0	0	0	0	0	0	No Level
4AI20EC076	Rudresh L S	P	0	0	0	9	0	0	0	0	0	0	0	2	11	Remember
4AI20EC077	Unnathi S V	P	0	0	0	4	8	2	0	0	0	5	5	0	24	Understand
4AI20EC078	Safa Ali	P	5	9	0	0	0	0	9	0	5	4	7	5	30	Understand
4AI20EC080	Sanmathi H M	P	1	0	0	0	0	0	8	0	3	4	0	2	12	Understand
4AI20EC081	Shabaz Khan	P	2	5	0	0	0	0	4	6	5	0	0	0	22	Understand
4AI20EC082	Shakthi B S	P	5	6	0	0	0	0	5	7	5	0	0	0	28	Understand
4AI20EC083	Sheethal M	P	0	0	0	4	10	2	5	7	5	0	0	0	33	Understand
4AI20EC084	Shree Sameehana R	P	0	0	0	9	10	3	0	0	0	5	7	5	39	Understand
4AI20EC085	Shree Vishnu N V	P	0	0	0	3	7	1	0	0	0	6.5	5	3.5	26	Understand
4AI20EC086	Shreya B M	P	4	10	0	0	0	0	0	0	5	0	0	5	19	Understand
4AI20EC087	Shwetha H S	P	0	0	0	7	10	2	0	0	0	10	7	4	40	Understand
4AI20EC088	Sneha N S	P	0	0	0	7	9.5	3.5	0	0	0	9	10	5	44	Understand
4AI20EC089	Sonika H P	P	0	0	0	0	10	0	0	0	0	7	9	4	30	Understand
4AI20EC090	Spoorthi D N	P	0	0	0	2	6	3	0	0	0	8	8	3	30	Understand

			Reverse: MOV R3 , #00 MOV R4 , #08 — Counter intitialized to number of bits Back: MOV A , R1 — Number moved to A from R1 RLC A — Rotate left through carry so that MSB is moved to carry MOV R1 , A — Save the rotated number MOV A , R3 — Move number from R3 to A RRC A — Rotate right trough carry so that carry is moved to MSB MOV R3 , A — Save the rotated number DJNZ R4 , Back — DECREMENT THE COUNTER, repeat until R4≠0 MOV A , R3 — When R4=0, Copy reversed number into A RET — Return to main program END **Program with Comments - 6+4 = 10Marks**			
	c	**Write an assembly language program with proper logical comments to add an array of six 8-bit numbers starting from address 9000H and store the result in 900AH.**	CO2	L2	05

Label	Opcode	Operands	Comments
	ORG	0000H	
	MOV	DPTR , #9000H	
	MOV	R_1 , #06H	Initialize counter
	CLR	C	Clear carry
	MOV X	A , @DPTR	Copy 1st number to A
	MOV	R2 , A	Save it in R2
	MOV	R_3 , #00	R3 to hold carry
	MOV	R0, #00	Register to hold the sum
Back:	MOV	A,R0	Initially sum=0
	ADD	A, R2	Add data in A with data in R2 and Sum is in A
	MOV	R0, A	Move sum to R0
	JNC	Next	If Carry=0, jump to Next
	INC	R_3	If Carry =1 Increment r3
Next:	INC	DPTR	Increment pointer
	MOVX MOV	A,@DPTR R2,A	Copy next number to A Save it in R2
	DJNZ	R_1 , Back	Decrement counter, if R1≠0, jump to back else
	MOV	DPTR, #900AH	To store sum at 900A
	MOV	A, R0	Copy sum in R0 to A
	MOV X	@DPTR, A	Move sum to location 900A
	INC	DPTR	Increment pointer
	MOV	A,R3	Save carry bit into next location
	MOV X	@DPTR, A	
Here:	SJMP	Here	
	END		

Program with Comments - 6+4 = 10Marks

		OR			
2	a	**What is a subroutine and explain the instructions related to subroutine in 8051.** • Subroutines are often used to *perform tasks that need to be performed frequently* • This makes a program more *structured* in addition to *saving memory space*	CO2	L1	10

2 Scheme of Evaluation

Date: 02/08/2022 | **AIT, E&C Dept** | **Test: 2**
Time: 12-1 PM | **Sub: 8051 Microcontrollers (18EC46)** | **Marks: 50**
Answer one full question from each part

Q.No		PART A	CO	BT/CL	marks
1	a	**Explain the following instructions with suitable examples:** **(i) DA A (ii) SWAP A (iii) XCHD A, SRC (iv) ANL A, R1 (v) SETB 00h**	CO2	L1	10
		2 Marks for each with example = 2M x 5 = 10M (i) DA A ;decimal adjust for addition • The "DA" instruction works only on A. • In other word, while the source can be an operand of any addressing mode, the destination must be in register A in order for DA to work. • After an ADD or ADDC instruction ▪ If the lower nibble (4 bits) is greater than 9, or if AC=1, add 0110 to the lower 4 bits ▪ If the upper nibble is greater than 9, or if CY=1, add 0110 to the upper 4 bits (ii) SWAP A • It swaps the lower nibble and the higher nibble • In other words, the lower 4 bits are put into the higher 4 bits and the higher 4 bits are put into the lower 4 bits • SWAP works only on the accumulator (A) (iii) XCHD A, SRC • Exchange lower nibble between A and the source operand • the upper nibble of A and the upper nibble of the address location in Rp do not change. (iv) ANL A, R1 • This instruction will perform a logic AND on the two operands and place the result in the destination • The destination is normally the accumulator • The source operand can be a register, in memory, or immediate (v) SETB 00h Set the bit (bit = 1) addressed at 00h. In other words, the bit 0 of the register R0 is to be set.			
	b	**Write an assembly language program with proper logical comments to check whether the given byte is bitwise palindrome or not using subroutine. If palindrome store FFH otherwise store 00H.**	CO2	L2	10

Label	Opcode	Operands	Comments
	ORG	0000H	
	MOV	DPTR , #9000H	Initialize DPTR to 9000h – number is in 9000H
	MOVX	A , @DPTR	Copy number to A
	MOV	R1 , A	Save a copy in R1 and R2
	MOV	R2 , A	
	MOV	R3 , #00	R3 is used to store the reversed number
	ACALL CJNE	Reverse A , R2 , NOT_P	Call the subroutine Compare reversed no. in A with the original number. If not equal then jump
	MOV	A , #0FFH	If equal copy FFh into A
	SJMP	Last	
NOT_P:	MOV	A , # 00	If not equal store 00h in A
	INC	DPTR	Increment DPTR
	MOVX	@DPTR , A	Store the result in external memory addressed by DPTR
Last:	SJMP	Last	

	CLR	C	Clear carry bit
Back:	ACALL	ADDT	Call the subroutine
	INC	R0	Increments the pointers
	INC	R1	
	INC	DPTR	
	DJNZ	R4, Back	Decrement the counter
Here:	SJMP	Here	
ADDT:	MOV	A, @R0	Adds the byte of 2 numbers along with carry
	ADDC	A, @R1	
	MOVX	@DPTR, A	Store the sum
	RET		
	END		

Program with Comments - 6+4 = 10Marks

c	Explain the difference between the following instructions: (i) JNC and JNZ (ii) RRC A and RR A	CO2	L2	05

(i) JNC and JNZ -2.5 M

JNZ label

- Checks whether the content of Accumulator ≠0 and if true, jumps to the label specified in the instruction else executes the next instruction
- Does not check the status of the flag register.
- Usually followed by the instruction that has Accumulator as one of the operand.

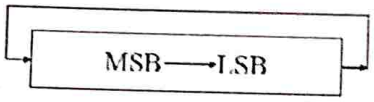
JNC label

- Checks if Carry flag ≠ 0 and if true, jumps to the label specified in the instruction else executes the next instruction.
- Checks the status of the flag register.
- Usually followed by the instructions ADD, ADDC, SUBB and CJNE.

(ii) RRC A and RR A - 2.5 M

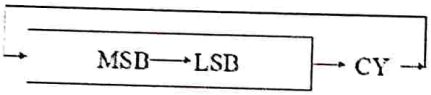
RR A

Rotates the contents of Accumulator right by one bit.
8 bits are involved in the shifting.



RRC A

Rotates the contents of Accumulator right through carry.
9 bits are involved in the shifting.



		PART B			
3	a	Interface 8 switches to port1 and 8 LEDs to port 0 and write a program to input the switch status and display on LEDs.	CO4	L2	10

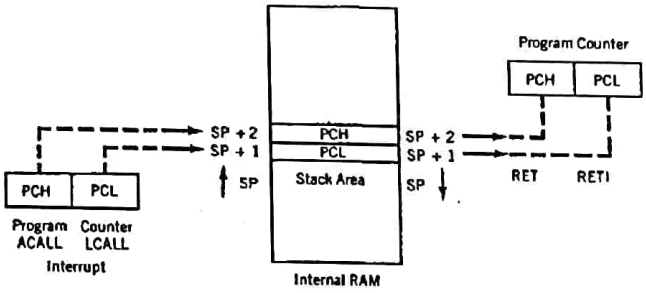
- When a subroutine is called, *control is transferred* to that subroutine, the processor ***saves*** on the stack the address of the instruction immediately below the LCALL and begins to fetch instructions from the ***new location***
- After finishing execution of the subroutine the instruction **RET *transfers control back*** to the caller
- Every subroutine ***needs*** RET as the last instruction

LCALL (long call)
LCALL ladd – Calls the subroutine located anywhere in program memory space; push the address of the instruction immediately following the call on the stack.
o 3-byte instruction
o First byte is the opcode
o Second and third bytes are used for address of target subroutine. Subroutine is located anywhere within 64K byte address space.

ACALL (absolute call)
ACALL sadd – Calls the subroutine located on the same page as the address of the opcode immediately following the ACALL ; push the address of the instruction immediately following the call on the stack.
o 2-byte instruction
o 11 bits are used for address within 2K-byte range.

RET – Return to main program
Pops 2byte of data from the top of the stack into the program counter.

The only difference between ACALL and LCALL is
o The target address for LCALL can be anywhere within the 64K byte address
o The target address of ACALL must be within a 2K-byte range
The use of ACALL instead of LCALL can save a number of bytes of program ROM space.



Definition – 4M
3 INSTRUCTIONS 2 MARKS EACH = 3X2 = 6M

b	**Write an assembly language program with proper logical comments to add 2 multibyte numbers using subroutine.**	**CO2**	**L2**	**10**

Label	Opcode	Operands	Comments
	ORG	0000H	
	MOV	DPTR , #9000H	Address to store sum
	MOV	R0 , #30H	Starting address of first multibyte no.
	MOV	R1 , #40H	Starting address of second multibyte no.
	MOV	R4 , #04	Counter for no. of additions

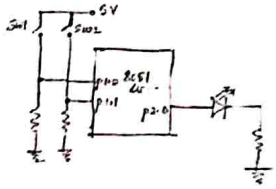
	c	**Write a program to perform the following:** **(a) Keep monitoring the P1.2 bit until it becomes high (b) When P1.2 becomes high, write value 45H to port 0 (c) Send a high-to-low (H-to-L) pulse to P2.3**	CO4	L2	05

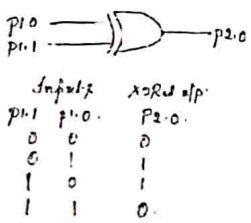
```
        SETB P1.2          ;make P1.2 an input
        MOV  A,#45H        ;A=45H
AGAIN:  JNB  P1.2,AGAIN    ;get out when P1.2=1
        MOV  P0,A          ;issue A to P0
        SETB P2.3          ;make P2.3 high
        CLR  P2.3          ;make P2.3 low for H-to-L
```

Program with Comments – 5

OR

4	a	**Interface to 8051 i) Two switches sw1 & sw2 to port pins p2.0 & p2.1 ii) One LED to p1.0 and write ALP to realize 2 input XOR operation.**	CO4	L2	10



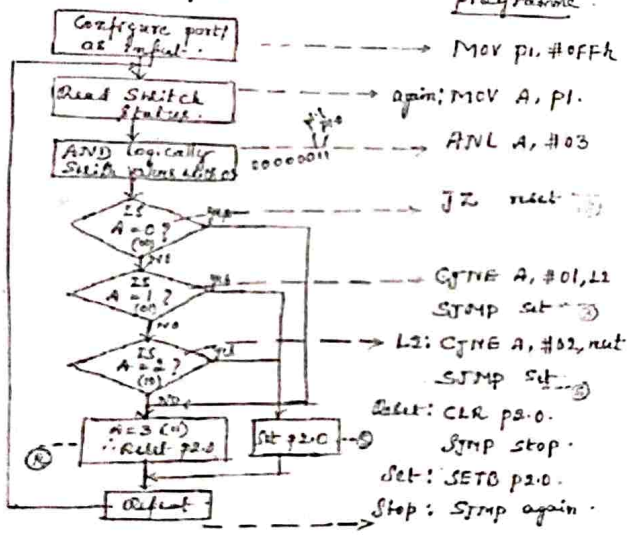


Inputs		XORed o/p
P1.1	P1.0	P2.0
0	0	0
0	1	1
1	0	1
1	1	0

FIGURE WITH EXPLANATION -4M

PROGRAM – 6M

Flow diagram to realize XOR operation.



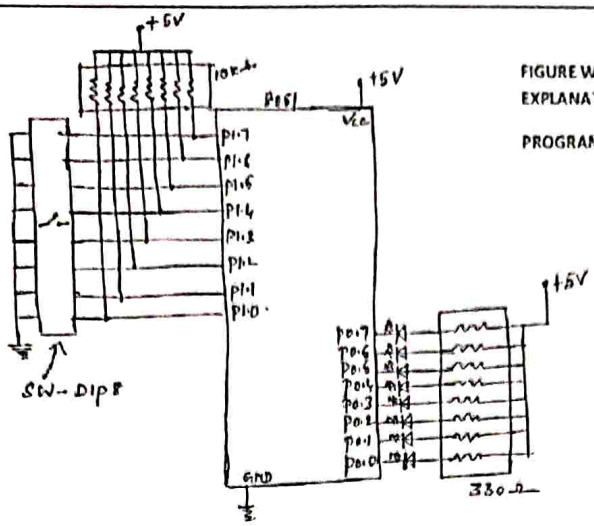


FIGURE WITH EXPLANATION -5M

PROGRAM – 5M

programme

```
MOV A, #0FFH  ; now A = FFh
MOV P1, A     ; make P1 as input port.
                by writing all 1's.
back: MOV A, P1  ; get the data from port1
MOV P0, A     ; Send it to port0.
SJMP back     ; Repeat the process. This P1
                Read the switch status & o/p that
                data in port 0.
```

b	**Write an assembly language program with proper logical comments to find whether the data 7Fh is positive or negative. If positive store FFh in register R1 else store 00 at same location. Explain with suitable example.**	**CO1**	**L2**	**10**

Label	Opcode	Operands	Comments
	ORG	0000H	
	MOV	A, #7FH	
	RLC JC	A NEG	MSB is moved to Carry If MSB =1 , It is negative
	MOV	R1,#0FFH	If MSB =0, then given number is Positive Store FFh in R1
	SJMP	Here	
NEG:	MOV	R1,#00H	Store 00 in R1 if negative
Here:	SJMP	Here	
	END		

Program with Comments – 7 EXAMPLE -3M

Q.No			Max Marks	CO	BT/CL
1a		*Explain the function of each bit of TMOD & TCON registers in 8051.*	10	3	L2
1b		*Write an ALP with proper logical comments, to generate a square wave of frequency 2 kHz, on port pin P1.0 (LSB of port1). Use timer 0 in mode 2 (8 bit auto reload mode). Assume crystal =11.0592 MHz.*	10	3	L2
1c		*Explain timer/counter action in Mode 1 with a neat diagram.*	5	3	L2

b	Write an assembly language program with proper logical comments to convert hexadecimal number to ASCII. Explain the program with suitable example.	CO2	L2	10

Label	Opcode	Operands	Comments
	ORG	0000H	
	MOV	DPTR,#9000H	//ASCII no. to be converted to decimal
	MOVX	A,@DPTR	
	CJNE	A, #09, Next	
	AJMP	Last	(A) = 09
Next:	JC	Last	(A) < 09
	ADD	A, #07	(A) > 09 , Add 07h
Last:	ADD	A,#30H	Add 30h
	INC	DPTR	
	MOVX	@DPTR, A	
Here :	SJMP	Here	
	END		

Program with Comments - 7 EXAMPLE -3M

c	A switch is connected to pin P1.7. Write a program to check the status of SW and perform the following: (a) If SW=0, send letter 'N' to P2 (b) If SW=1, send letter 'Y' to P2	CO4	L2	05

```
        SETB    P1.7        ;make P1.7 an input
AGAIN:  JB      P1.7,OVER   ;jump if P1.7=1
        MOV     P2,#'N'     ;SW=0, issue 'N' to P2
        SJMP    AGAIN       ;keep monitoring
OVER:   MOV     P2,#'Y'     ;SW=1, issue 'Y' to P2
        SJMP    AGAIN       ;keep monitoring
```

Program with Comments - 5

Internal : 3

Semester:4-CBCS 2018

Subject : MICROCONTROLLER (18EC46)

Faculty : Divya

Date : 29/08/2022

Time : 12:00 - 13:00

Max Marks: 50

Part A
Answer any 1 questions

3a		*Explain the interrupts of 8051 & explain IP and IE registers of 8051.*	10	3	L2
3b		*With a neat diagram show how a stepper motor is interfaced to 8051. Write an assembly language program to rotate it continuously.*	10	4	L2
3c		*Draw the interfacing circuit of 8051 with LCD and explain the functional pins of LCD.*	5	4	L2

2a		*Explain the functions of the RS-232 DB-9 connector pins & explain how 8051 transmits & receives a character serially using the UART.*	10	3	L2
2b		*Write a program with proper comments to transfer the message 'GOOD LUCK" serially at 9600 baud rate, 8 bit data, 1 stop bit. Do this continuously.*	10	3	L2
2c		*Explain the steps involved in executing an interrupt using 8051 microcontroller.*	5	3	L2
Part B					
Answer any 1 questions					
Q.No			**Max Marks**	**CO**	**BT/CL**

ADICHUNCHANAGIRI INSTITUTE OF TECHNOLOGY

Department of Electronics & Communication Engineering (EC)

Evaluation

USN	Name	Present (P) / Absent (Ab)	Q1			Q2			Q3			Q4			IA Total	BT/CL
			a	b	c	a	b	c	a	b	c	a	b	c		
4AI20EC057	Nirupam Hegde M P	P	1	0	0	0	8	4	2	9	0	0	0	0	23	Understand
4AI20EC058	Nisarga S	P	8	9	5	0	0	0	2	10	4	0	0	0	38	Understand
4AI20EC059	Nisarga Kanth K L	P	8	8	5	0	0	0	0	8	4	0	0	0	33	Understand
4AI20EC060	Nischitha C V	P	5	8	3.5	0	0	0	0	0	0	1	9.5	4	31	Understand
4AI20EC061	Nischitha H S	P	5.5	9	4.5	0	0	0	0	0	0	9	8	4	40	Understand
4AI20EC062	Nithin H M	P	10	9	5	0	0	0	0	0	0	9.5	9.5	4	47	Understand
4AI20EC063	Nithin N	P	3	0	3	0	0	0	0	0	0	8	0	0	14	Understand
4AI20EC064	Sai Geethika P V	P	9.5	9.5	5	0	0	0	0	0	0	10	9.5	4.5	48	Understand
4AI20EC065	Pallavi S	P	6.5	0	4	0	0	0	0	8.5	4	0	0	4	23	Understand
4AI20EC066	Pooja Manjunath Naik	P	10	9.5	5	0	0	0	0	0	0	9.5	10	4	48	Understand
4AI20EC067	Poojashree M N	P	8	9	4	0	0	0	0	0	0	9	5	2	37	Understand
4AI20EC068	Pragathi S	P	8	9	4	0	0	0	5	10	3	0	0	0	39	Understand
4AI20EC069	Prajwal S L	P	0	0	0	0	8	0	0	0	0	9	0	3	20	Understand
4AI20EC070	Praneetha K	P	8	9	5	0	0	0	5	9	3	0	0	0	39	Understand
4AI20EC071	Preksha C Y	P	2	1	2	0	0	0	0	0	0	10	0	0	15	Understand
4AI20EC072	Prathik R	P	9	0	3	0	0	0	8	9	0	9	7	2	30	Understand
4AI20EC073	Rahul B N	P	7	9	4	0	0	0	0	0	0	8	5	4	37	Understand
4AI20EC074	Rakshith K	P	0	0	0	0	9	4	0	0	0	9	0	0	22	Understand
4AI20EC075	Rakshith N P	P	5	6	0	0	0	0	0	0	0	5	4	5	25	Understand
4AI20EC076	Rudresh L S	P	0	0	0	0	3	4	0	5	0	7	7	3	24	Understand
4AI20EC077	Unnathi S V	P	7	5	4	0	0	0	6	8	4	0	0	0	34	Understand
4AI20EC078	Safa Ali	P	4	4	0	0	0	0	0	0	0	0	6	0	14	Understand
4AI20EC080	Sanmathi H M	P	0	1	0	0	0	0	6	2	5	0	5	0	14	Understand
4AI20EC081	Shabaz Khan	P	0	0	0	0	7	2	0	0	0	0	0	3	12	Understand
4AI20EC082	Shakthi B S	P	0	0	0	0	8	2	7	10	0	0	0	0	27	Understand
4AI20EC083	Sheethal M	P	0	7	4	0	0	0	0	0	0	10	0	4	25	Understand
4AI20EC084	Shree Sameehana R	P	0	0	0	5	9	5	0	0	0	10	10	5	44	Understand
4AI20EC085	Shree Vishnu N V	P	0	0	0	0	9	2	7	10	0	0	0	0	28	Understand
4AI20EC086	Shreya B M	P	4	9	5	0	0	0	10	10	0	0	0	0	38	Understand
4AI20EC087	Shwetha H S	P	9	9	4.5	0	0	0	0	0	0	9	10	4.5	46	Understand
4AI20EC088	Sneha N S	P	8	8	5	0	0	0	0	0	0	9	10	4	44	Understand
4AI20EC089	Sonika H P	P	0	0	0	0	9	4	0	0	0	10	0	3	26	Understand
4AI20EC090	Spoorthi D N	P	9	0	5	0	0	0	0	0	0	0	8	4	26	Understand

4a		*Write a C program that continuously gets a single bit of data from P1.7 and sends it to P1.0, while simultaneously creating a square wave of 200 s period on pin P2.5. Use Timer 0 to create the square wave. Assume that XTAL = 11.0592 MHz.*	10	3	L2
4b		*Interface 8051microcontroller to DAC0808 and write an ALP to generate the sine wave by showing the calculation.*	10	4	L2
4c		*Write an assembly language program to rotate a motor 180 degree in clockwise direction. The motor has a step angle of 1.8 degree. Also write the 4 step sequence table.*	5	4	L2

2 Scheme of Evaluation

Date: 29/08/2022
Time: 12-1 PM

AIT, E&C Dept
Sub: 8051 Microcontrollers (18EC46)
Answer one full question from each part

Test: 3
Marks: 50

PART A

Answer any1 question(s)

Q.No			Marks	CO	BT/ CL
1	a	Explain the function of each bit of TMOD & TCON registers in 8051.	10	CO3	L2

Sol:

(MSB) GATE | C/T | M1 | M0 — Timer1 ; GATE | C/T | M1 | M0 — Timer0 (LSB)

M1	M0	Mode	Operating Mode
0	0	0	13-bit timer mode 8-bit timer/counter THx with TLx as 5-bit prescaler
0	1	1	16-bit timer mode 16-bit timer/counter THx and TLx are cascaded; there is no prescaler
1	0	2	8-bit auto reload 8-bit auto reload timer/counter; THx holds a value which is to be reloaded TLx each time it overfolws
1	1	3	Split timer mode

Gating control when set. Timer/counter is enable only while the INTx pin is high and the TRx control pin is set
When cleared, the timer is enabled whenever the TRx control bit is set

Timer or counter selected
Cleared for timer operation (input from internal system clock)
Set for counter operation (input from Tx input pin)

TCON: Timer/Counter Control Register

TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0

The upper four bits are used to store the TF and TR bits of both timer 0 and 1

The lower 4 bits are set aside for controlling the interrupt bits

D7 ... D0

TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0

TF1	TCON.7	Timer 1 overflow flag. Set by hardware when timer/counter 1 overflows. Cleared by hardware as the processor vectors to the interrupt service routine
TR1	TCON.6	Timer 1 run control bit. Set/cleared by software to turn timer/counter 1 on/off
TF0	TCON.5	Timer 0 overflow flag. Set by hardware when timer/counter 0 overflows. Cleared by hardware as the processor vectors to the interrupt service routine
TR0	TCON.4	Timer 0 run control bit. Set/cleared by software to turn timer/counter 0 on/off
IE1	TCON.3	External interrupt 1 edge flag. Set by CPU when the external interrupt edge (H-to-L transition) is detected. Cleared by CPU when the interrupt is processed
IT1	TCON.2	Interrupt 1 type control bit. Set/cleared by software to specify falling edge/low-level triggered external interrupt
IE0	TCON.1	External interrupt 0 edge flag. Set by CPU when the external interrupt edge (H-to-L transition) is detected. Cleared by CPU when the interrupt is processed
IT0	TCON.0	Interrupt 0 type control bit. Set/cleared by software to specify falling edge/low-level triggered external interrupt

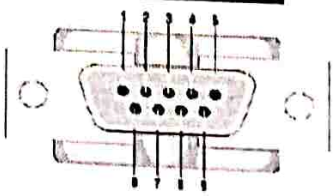
TMOD Reg – 5M TCON Reg – 5M

ADICHUNCHANAGIRI INSTITUTE OF TECHNOLOGY

Department of Electronics & Communication Engineering (EC)

USN	Name	Present (P) / Absent (Ab)	Q1			Q2			Q3			Q4			IA Total	BT/CL
			a	b	c	a	b	c	a	b	c	a	b	c		
4AI20EC091	Srujan K J	P	3	5	0	0	0	0	0	0	0	7	4	3	22	Understand
4AI20EC092	Srusti B A	P	9	8	4	0	0	0	7	10	0	0	0	0	38	Understand
4AI20EC093	Sudeep K P	P	0	0	0	0	5	0	0	0	0	7	7	3	22	Understand
4AI20EC094	Sugam Ganesh K S	P	3	4	0	0	0	0	0	0	0	0	0	0	7	No Level
4AI20EC095	Sugam K N	P	0	0	0	0	8	5	0	0	0	0	0	0	13	Understand
4AI20EC096	Sujay Urs C B	P	0	0	0	0	7	3	0	0	0	2	0	4	16	Understand
4AI20EC097	Sukhi D	P	8	8	3	0	0	0	0	0	0	1	10	4	34	Understand
4AI20EC098	Swamy Kotresh B	P	6	1	3	0	2	0	0	0	0	0	1	3	14	Understand
4AI20EC099	Swarna Gowri K S	P	0	0	0	1	9	3	0	0	0	10	8	4	35	Understand
4AI20EC100	Swathi B P	P	5	9	3	0	0	0	1	10	4	0	4	1	32	Understand
4AI20EC101	Swathisha H Shetty	P	2	4	0	0	0	0	0	5	0	7	3	0	16	Understand
4AI20EC102	Vagdevi M K	P	0	0	0	3	7	5	0	0	0	8	4	2	29	Understand
4AI20EC103	Vaishnavi S R	P	10	8	5	0	0	0	0	0	0	10	10	0	43	Understand
4AI20EC104	Varsha C J	P	8	8	5	0	0	0	0	0	0	1	10	4	36	Understand
4AI20EC105	Varshini S	P	8	8	4	0	0	0	0	7	2	0	0	0	29	Understand
4AI20EC106	Varshith D N	P	6	8	0	0	0	0	0	0	0	10	8	3	35	Understand
4AI20EC107	Varshitha S V	P	9	9	4	0	0	0	0	0	0	8	9	3	42	Understand
4AI20EC108	Vedhashree C R	P	4	5	0	0	0	0	0	0	0	0	0	2	11	Understand
4AI20EC109	Vinayak Bhyresh Onimani	P	7	9	0	0	0	0	0	0	0	0	0	0	16	Understand
4AI20EC110	Vinayaka M S	P	0	0	0	0	6	2	0	0	0	0	0	4	12	Understand
4AI20EC111	Vivek S M	P	10	10	5	0	0	0	10	10	5	0	0	0	50	Understand
4AI20EC112	Yashwanth K N	P	8	9	2	0	0	0	0	0	0	8	3	3	33	Understand
4AI20EC113	Yogish N S	P	0	0	0	1	6	0	0	0	0	9	3	3	22	Understand
4AI21EC402	Nandashree A G	P	7	7	4	0	0	0	0	6	5	0	0	0	29	Understand
4AI21EC403	Sahana K R	P	6	0	3	0	0	0	0	0	0	0	4	3	16	Understand

RS232 Connector DB-9



RS232 DB-9 Pins

Pin	Description
1	Data carrier detect (-DCD)
2	Received data (RxD)
3	Transmitted data (TxD)
4	Data terminal ready (DTR)
5	Signal ground (GND)
6	Data set ready (-DSR)
7	Request to send (-RTS)
8	Clear to send (-CTS)
9	Ring indicator (RI)

RS232

FIGURE WITH EXPLANATION -5M

- DTE (data terminal equipment) refers to terminal and computers that send and receive data
- DCE (data communication equipment) refers to communication equipment, such as modems, that are responsible for transferring the data.
- The simplest connection between a PC and microcontroller requires a minimum of three pins: TxD, RxD and ground.

❑ **DTR (data terminal ready)**

➢ When terminal is turned on, it sends out signal DTR to indicate that it is ready for communication.

❑ **DSR (data set ready)**

➢ When DCE is turned on and has gone through the self-test, it asserts DSR to indicate that it is ready to communicate.

❑ **RTS (request to send)**

➢ When the DTE device has byte to transmit, it asserts RTS to signal the modem that it has a byte of data to transmit.

❑ **CTS (clear to send)**

➢ When the modem has room for storing the data it is to receive, it sends out signal CTS to DTE to indicate that it can receive the data now.

❑ **DCD (data carrier detect)**

➢ The modem asserts signal DCD to inform the DTE that a valid carrier has been detected and that contact between it and the other modem is established.

❑ **RI (ring indicator)**

➢ An output from the modem and an input to a PC indicates that the telephone is ringing.

➢ It goes on and off in synchronous with the ringing sound.

The following are the steps to program the 8051 to transfer character bytes serially.

1. **TMOD** register is loaded with the value **20H**, indicating the use of timer 1 in mode 2 (8-bit auto-reload) to set baud rate.
2. The **TH1** is loaded with one of the values to set baud rate for serial data transfer .
3. The **SCON** register is loaded with the value **50H**, indicating serial mode 1, where an 8 - bit data is framed with start and stop bits.
4. **TR1** is set to 1 to start timer 1.
5. TI is cleared by **CLR TI** instruction.
6. The character byte to be transferred serially is written into **SBUF** register.
7. The TI flag bit is monitored with the use of instruction "**JNB TI, xx**" to see if the character has been transferred completely.
8. To transfer the next byte, go to step 5.

The following are the steps to program the 8051 to receive character bytes serially.

1. **TMOD** register is loaded with the value **20H**, indicating the use of timer 1 in mode 2 (8-bit auto-reload) to set baud rate.
2. TH1 is loaded to set baud rate.
3. The **SCON** register is loaded with the value **50H**, indicating serial mode 1, where an 8- bit data is framed with start and stop bits.
4. TR1 is set to 1 to start timer 1. **SETB TR1**
5. RI is cleared by **CLR RI** instruction.

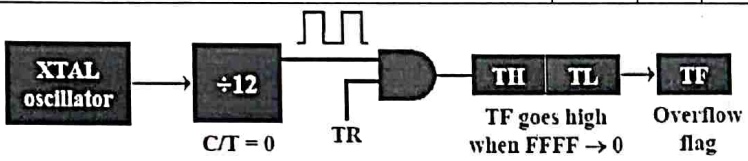
	b	Write an ALP with proper logical comments, to generate a square wave of frequency 2 kHz, on port pin P1.0 (LSB of port1). Use timer 0 in mode 2 (8 bit auto reload mode). Assume crystal = 11.0592 MHz.	10	CO3	L2

(a) T = 1 / f = 1 / 2 kHz = 500 us the period of square wave.
(b) 1 / 2 of it for the high and low portion of the pulse is 250 µs.
(c) 250 µs / 1.085 µs = 230 and 256 - 230 = 26 which in hex is 1AH.
(d) TH = 1A in hex. The program is as follows. } 5M

```
        MOV TMOD,#02H ;Timer 0, 16-bitmode
AGAIN:  MOV TH0,#1AH ; TH0=1A, the high byte of timer
        SETB TR0 ;Start timer 1
BACK:   JNB TF0,BACK ;until timer rolls over
        CLR TR0 ;Stop the timer 1
        CLR P1.0 ;Clear timer flag 1
        CLR TF0 ;Clear timer 1 flag
        SJMP AGAIN ;Reload timer
```

PROGRAM WITH COMMENTS – 5M

	c	Explain timer/counter action in Mode 1 with a neat diagram.	5	CO3	L2



The following are the characteristics and operations of mode 1:

1. It is a 16-bit timer; therefore, it allows value of 0000 to FFFFH to be loaded into the timer's register TL and TH
2. After TH and TL are loaded with a 16-bit initial value, the timer must be started.
   - This is done by **SETB TR0** for timer 0 and **SETB TR1** for timer 1
3. After the timer is started, it starts to count up.
   - It counts up until it reaches its limit of FFFFH. When it rolls over from FFFFH to 0000, it sets high a flag bit called **TF (timer flag)**
     - ✓ Each timer has its own timer flag: TF0 for timer 0, and TF1 for timer 1.
     - ✓ This timer flag can be monitored
   - When this timer flag is raised, one option would be to stop the timer with the instructions **CLR TR0 or CLR TR1**, for timer 0 and timer 1, respectively
4. After the timer reaches its limit and rolls over, in order to repeat the process **TH and TL must be reloaded** with the original value, and **TF must be reloaded to 0.**

FIGURE – 2M EXPLANATION -3M

2	a	Explain the functions of the RS-232 DB-9 connector pins & explain how 8051 transmits & receives a character serially using the UART.	10	CO3	L2

Upon activation of an interrupt, the microcontroller goes through the following steps

1. It finishes the instruction it is executing and saves the address of the next instruction (PC) on the stack.
2. It also saves the current status of all the interrupts internally (i.e: not on the stack).
3. It jumps to a fixed location in memory, called the interrupt vector table, that holds the address of the ISR.
4. The microcontroller gets the address of the ISR from the interrupt vector table and jumps to it.
   - ▶ *It starts to execute the interrupt service subroutine until it reaches the last instruction of the subroutine which is RETI (return from interrupt).*
5. Upon executing the RETI instruction, the microcontroller returns to the place where it was interrupted.
   - ▶ *First, it gets the program counter (PC) address from the stack by popping the top two bytes of the stack into the PC. Then it starts to execute from that address.*

STEPS – 5M

PART B

Answer any1 question(s)

Q.No			Marks	CO	BT/CL
3	a	**Explain the interrupts of 8051 & explain IP and IE registers of 8051.**	10	CO3	L2

- ▶ An interrupt is an external or internal event that interrupts the microcontroller to inform it that a device needs its service.

❑ Interrupts

- Whenever any device needs its service, the device notifies the microcontroller by sending it an interrupt signal.
- Upon receiving an interrupt signal, the microcontroller interrupts whatever it is doing and serves the device.
- The program which is associated with the interrupt is called the interrupt service routine (ISR) or interrupt handler.

Six interrupts are allocated as follows.

1. Reset – power-up reset.
2. Two interrupts are set aside for the timers: one for timer 0 and one for timer 1.
3. Two interrupts are set aside for hardware external interrupts.
   - P3.2 and P3.3 are for the external hardware interrupts INT0 (or EX1), and INT1 (or EX2).
4. Serial communication has a single interrupt that belongs to both receive and transfer.

- ▶ **Upon reset, all interrupts are disabled (masked), meaning that none will be responded to by the microcontroller if they are activated.**
- ▶ **The interrupts must be enabled by software in order for the microcontroller to respond to them.**
- ▶ **Register called IE (interrupt enable) is responsible for enabling (unmasking) and disabling (masking) the interrupt.**

6. The RI flag bit is monitored with the use of instruction "JNB RI, xx" to see if an entire character has been received yet.
7. When RI is raised, SBUF has the byte, its contents are moved into a safe place.
8. To receive the next character, go to step 5.

SERIAL TRANSMISSION – 2.5M SERIAL RECEPTION – 2.5M

	b	Write a program with proper comments to transfer the message "GOOD LUCK" serially at 9600 baud rate, 8 bit data, 1 stop bit. Do this continuously.	10	CO3	L2

```
#include <reg51.h>
void main (void)
{
  unsigned char z;
  unsigned char msg[] = "GOOD LUCK";
  TMOD = 0X20;
  TH1 = 0XFF;
  SCON = 0X50;
  TR1 = 1;

  for (z=0; z<9;z++)
  {
    SBUF = msg[z];
    while(TI==0)
      TI = 0 ;
  }
}
```

PROGRAM WITH COMMENTS – 10M

OR

```
        ORG 0000
        MOV TMOD, #20H
        MOV TH, #-3
        MOV SCON, #50H
        SETB TR1
BACK : MOV DPTR, # MESS1
AGAIN: CLR A
        MOVC A, @A+DPTR
        JZ BACK
        MOV SBUF, A
HERE: JNB TI, HERE
        CLR TI
        INC DPTR
        SJMP AGAIN

MESS1 : DB "GOOD LUCK", 0
        END
```

	c	Explain the steps involved in executing an interrupt using 8051microcontroller.	5	CO3	L2

Label	Opcode	Operands	Comments
	ORG	0000H	
MAIN:	MOV	R0, #04H	
	MOV	A, #01H	// MOV A, #08H for Anticlockwise rotation
RPT:	MOV	P0, A	
	RL	A	// RR A for Anticlockwise rotation
	CALL	DELAY	
	DJNZ	R0, RPT	
	JMP	MAIN	
DELAY:	MOV	R1, #0FFH	
LP2:	MOV	R2, #0FFH	
LP1:	DJNZ	R2, LP1	
	DJNZ	R1, LP2	
	RET		
	END		

	c	Draw the interfacing circuit of 8051 with LCD and explain the functional pins of LCD.	5	CO4	L2

INTERFACING CIRCUIT - 5M

EXPLANATION OF LCD PINS - 5M

Pin Descriptions for LCD

Pin	Symbol	I/O	Description
1	V_{SS}	–	Ground
2	V_{CC}	–	+5V power supply
3	V_{EE}	–	Power supply to control contrast
4	RS	I	RS = 0 to select command register, RS = 1 to select data register
5	R/W	I	R/W = 0 for write, R/W = 1 for read
6	E	I/O	Enable
7	DB0	I/O	The 8-bit data bus
8	DB1	I/O	The 8-bit data bus
9	DB2	I/O	The 8-bit data bus
10	DB3	I/O	The 8-bit data bus
11	DB4	I/O	The 8-bit data bus
12	DB5	I/O	The 8-bit data bus
13	DB6	I/O	The 8-bit data bus
14	DB7	I/O	The 8-bit data bus

D7 D0

EA	--	ET2	ES	ET1	EX1	ET0	EX0

EA (enable all) must be set to 1 in order for rest of the register to take effect

EA	IE.7	Disables all interrupts
--	IE.6	Not implemented, reserved for future use
ET2	IE.5	Enables or disables timer 2 overflow or capture interrupt (8952)
ES	IE.4	Enables or disables the serial port interrupt
ET1	IE.3	Enables or disables timer 1 overflow interrupt
EX1	IE.2	Enables or disables external interrupt 1
ET0	IE.1	Enables or disables timer 0 overflow interrupt
EX0	IE.0	Enables or disables external interrupt 0

Highest To Lowest Priority	
External Interrupt 0	(INT0)
Timer Interrupt 0	(TF0)
External Interrupt 1	(INT1)
Timer Interrupt 1	(TF1)
Serial Communication	(RI + TI)

- When the 8051 is powered up, the priorities are assigned according to the above table:
- We can alter the sequence of interrupt priority by assigning a higher priority to any one o the interrupts by programming a register called IP (interrupt priority).

D7 D0

--	--	PT2	PS	PT1	PX1	PT0	PX0

--	IP.7	Reserved
--	IP.6	Reserved
PT2	IP.5	Timer 2 interrupt priority bit (8052 only)
PS	IP.4	Serial port interrupt priority bit
PT1	IP.3	Timer 1 interrupt priority bit
PX1	IP.2	External interrupt 1 priority bit
PT0	IP.1	Timer 0 interrupt priority bit
PX0	IP.0	External interrupt 0 priority bit

Priority bit=1 assigns high priority
Priority bit=0 assigns low priority

INTERRUPTS OF 8051 – 3M

IP REG – 3.5M

IE REG – 3.5 M

	b	With a neat diagram show how a stepper motor is interfaced to 8051. Write an assembly language program to rotate it continuously.	10	CO4	L2

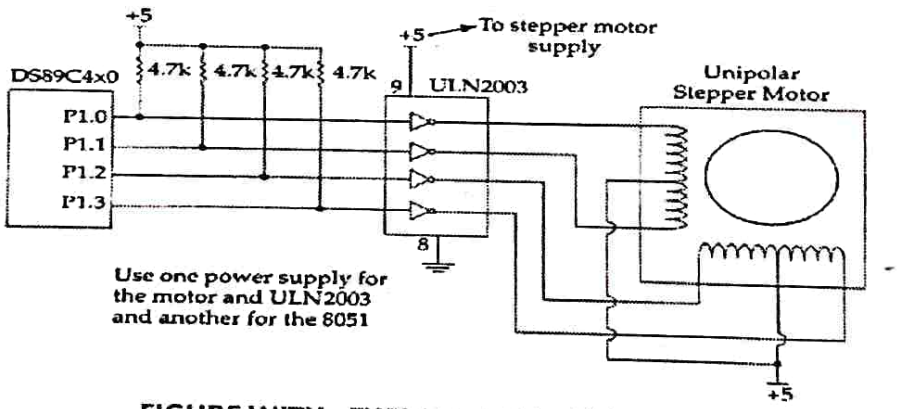
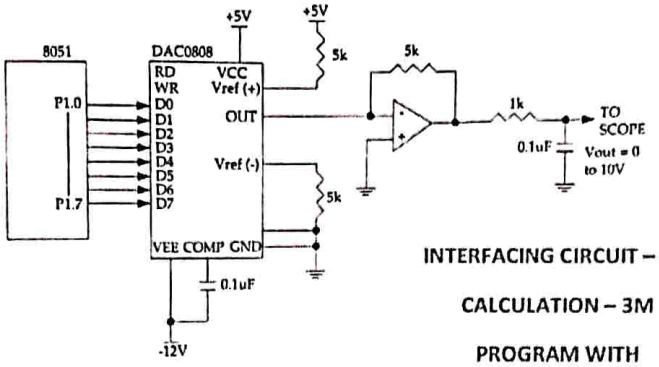


FIGURE WITH EXPLANATION - 5M

PROGRAM WITH COMMENTS - 5M

	b	Interface 8051microcontroller to DAC0808 and write an ALP to generate the sine wave by showing the calculation.	10	CO4	L2



INTERFACING CIRCUIT – 3M

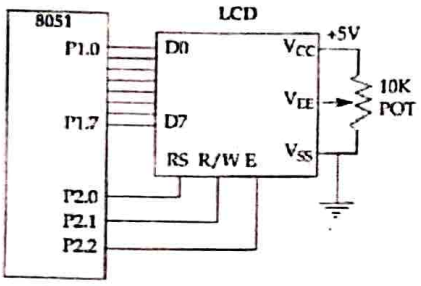
CALCULATION – 3M

PROGRAM WITH COMMENTS – 4M

Table 13-7: Angle vs. Voltage Magnitude for Sine Wave

Angle θ (degrees)	Sin θ	V_{out} (Voltage Magnitude) 5 V + (5 V × sin θ)	Values Sent to DAC (decimal) (Voltage Mag. × 25.6)
0	0	5	128
30	0.5	7.5	192
60	0.866	9.33	238
90	1.0	10	255
120	0.866	9.33	238
150	0.5	7.5	192
180	0	5	128
210	−0.5	2.5	64
240	−0.866	0.669	17
270	−1.0	0	0
300	−0.866	0.669	17
330	−0.5	2.5	64
360	0	5	128

```
AGAIN:  MOV   DPTR,#TABLE
        MOV   R2,#13
BACK:   CLR   A
        MOVC  A,@A+DPTR
        MOV   P1,A
        INC   DPTR
        DJNZ  R2,BACK
        SJMP  AGAIN
        ORG   300
TABLE:  DB    128,192,238,255,238,192
        DB    128,64,17,0,17,64,128
```

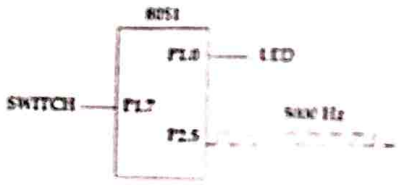


4	a	Write a C program that continuously gets a single bit of data from P1.7 and sends it to P1.0, while simultaneously creating a square wave of 200 µs period on pin P2.5. Use Timer 0 to create the squarewave. Assume that XTAL = 11.0592 MHz.	10	CO3	L2

Solution:

We will use timer 0 mode 2 (auto-reload). One half of the period is 100 µs. 100/1.085 µs = 92, and TH0 = 256 - 92 = 164 or A4H

```
#include <reg51.h>
sbit SW   =P1^7;
sbit IND  =P1^0;
sbit WAVE =P2^5;
void timer0(void) interrupt 1
{
  WAVE=~WAVE;  //toggle pin
}
void main()
{
  SW=1;          //make switch input
  TMOD=0x02;
  TH0=0xA4;      //TH0=-92
  IE=0x82;       //enable interrupt for timer 0
  while (1)
  {
    IND=SW;      //send switch to LED
  }
}
```



CALCULATION – 2M

PROGRAM WITH COMMENTS – 8M

	c	Write an assembly language program to rotate a motor 180 degree in clockwise direction. The motor has a step angle of 1.8 degree. Also write the 4 step sequence table.	5	CO4	L2

SOLUTION:

Step angle = 1.8^0

No. of steps for one complete rotation $= \frac{360^0}{1.8^0} = 200$

No. of steps required for 180^0 rotation $= \frac{200}{360^0} X\ 180^0 = 100_D = 64_H$

Wave Drive 4-Step Sequence

Clockwise	Step #	Winding A	Winding B	Winding C	Winding D	Counter-Clockwise
↓	1	1	0	0	0	↑
	2	0	1	0	0	
	3	0	0	1	0	
	4	0	0	0	1	

Label	Opcode	Operands	Comments
	ORG	0000H	
	MOV	R4, #19H	19H x 04 = 64H for 180^0
BACK:	MOV	R0, #04H	
	MOV	A, #08H	
RPT:	MOV	P0, A	
	RR	A	
	CALL	DELAY	
	DJNZ	R0, RPT	
	DJNZ	R4, BACK	
HERE:	SJMP	HERE	
DELAY:	MOV	R2, #0FFH	
LP2:	MOV	R3, #0FFH	
LP1:	DJNZ	R3, LP1	
	DJNZ	R2, LP2	
	RET		
	END		

CALCULATION - 1M

SEQUENCE TABLE – 1M

PROGRAM - 3M